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DISSERTATION

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MONOLITHIC SILICON PIXEL DETECTOR IN SOI TECHNOLOGY – DESIGN, REALIZATION AND CHARACTERIZATION

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Contents

List of Symbols

A	Atomic mass
C_{gs}	Small signal gate-source capacitance
C_{gd}	Small signal gate-drain capacitance
C_{int}	Integrating capacitance
C_{ox}	Gate oxide capacitance per unit area
c	Speed of light in vacuum
D_n	Electron diffusion constant
D_p	Hole diffusion constant
E	Electric field
E_c	Critical energy
E_{e-h}	Energy per electron-hole pair
E_g	Band gap energy
E_i	Intrinsic energy level
E_t	Trap energy levels in band gap
E_w	Weighting field
E_γ	Photon energy
F	Fano factor
f	Frequency
$G_{N_q \to V}$	Charge-to-voltage gain referred to the number of collected charge carriers
$G_{Q \to V}$	Charge-to-voltage gain referred to 1 fC charge
g_{ds}	Small signal transistor output conductance
g_m	Small signal transistor transconductance
g_{mb}	Small signal transistor bulk transconductance
I	Mean excitation energy
I_D	Transistor drain current

j_{diff}	Density of diffusion current
j_{gen}	Density of generation current
K'	Process current factor
k	Boltzman constant
L	Length of transistor channel
L_n	Diffusion length of electrons
L_p	Diffusion length of holes
M	Particle mass
m_e	Electron mass
N_0	Avogadro's number
N_A	Concentration of acceptor impurities
N_D	Concentration of donor impurities
N_t	Trap density
n_i	Intrinsic carrier concentration
p	Momentum
Q	Charge
Q_{coll}	Charge collected on detector electrode
q	Elementary charge
r_{ds}	Small signal transistor output resistance
r_e	Classical electron radius
T	Absolute temperature
T_{cut}	Cut-off energy
T_{max}	Maximum kinetic energy which can be imparted to a free electron in a single collision
t	Time
t_{int}	Integration time
V	Electrostatic potential
v	Particle speed
V_{bi}	Built-in voltage of semiconductor junction
V_{BS}	Transistor body-source voltage
V_{DET}	External reverse bias voltage applied to detector
V_{DS}	Transistor drain-source voltage
V_E	Early voltage
V_{GS}	Transistor gate-source voltage

V_T	Transistor threshold voltage
V_{T0}	Transistor threshold voltage at zero body-source voltage
V_{bs}	Small signal transistor bulk-source voltage
V_{gs}	Small signal transistor gate-source voltage
W	Width of transistor channel
W_n	Widths of depletion zone on the n side of a junction
W_p	Widths of depletion zone on the p side of a junction
W_d	Thickness detector depletion region
X_0	Radiation length
Z	Atomic number
z	Charge of particle
β	Relative particle speed
β'	Transistor current factor
γ	Relativistic dilatation factor
Δ	Energy loss
δ	Density effect correction
ε_0	Permittivity of free space
ε_{Si}	Silicon dielectric constant
μ	Charge carrier mobility
μ_e	Electron mobility
μ_h	Hole mobility
ν	Velocity of charge carrier
ν_e	Electron velocity
ν_h	Hole velocity
ν_{th}	Thermal velocity
ρ	Density
ρ_d	Charge density
σ_0	Capture cross-section of trap
τ_{eff}	Effective carrier trapping time
τ_g	Generation lifetime
τ_n	Electron lifetime in p-type region
τ_p	Hole lifetime in n-type region
Φ_w	Weighting potential

Chapter 1

Introduction

1.1 Background

The possibility of the detection of ionising radiation by a reverse biased semiconductor junction was first reported by McKay in 1951 [1]. Soon after the planar process had been introduced into the technology of semiconductor detectors [2], these devices became important tools of modern high energy physics, space science, medicine and many other disciplines. First silicon vertex detector was built in 1991 at the European Laboratory of Nuclear Physics CERN for the ALEPH experiment. The photograph of this system is presented in figure 1.1. It consisted of two layers of double-sided silicon strip detectors, arranged into concentric barrels around the beam pipe [3]. Due to the use of silicon detectors in this application, precise measurements of the trajectories of charged particles close to the interaction point could be provided.

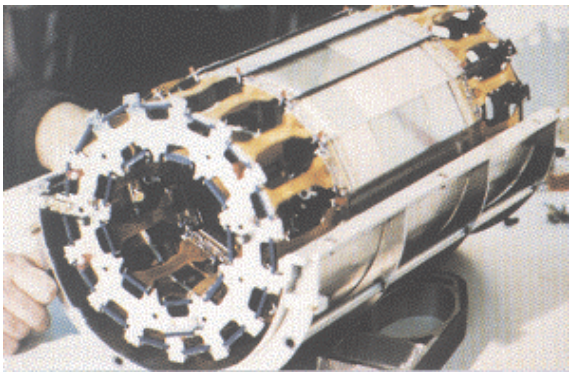


Figure 1.1: Photograph of the ALEPH vertex detector that was operated since 1991 [4].

For years, increasing demands of the high energy experiments and new areas of applications have been motivation for continuous development of new semiconductor detectors characterized by improved parameters in terms of granularity, charge collection time, readout speed, radiation hardness, small sensor perturbation to the particle trajectory and low cost. At present, existing solutions of active pixel detectors can be divided into two groups: hybrid and monolithic sensors. In the hybrid detectors, a matrix of radiation sensitive junctions and readout electronics are realized as separate entities, while in the monolithic detectors, both parts of the active sensor are integrated in one structure. Although most of the large scale applications of silicon detectors still bases on the hybrid approach, the development of the monolithic active pixel detectors becomes a common trend in the field of highly segmented ionising radiation sensors [5]. It is expected that the monolithic solutions will enable reducing material budget in future particle physics experiments and will allow lowering sensors costs due to the elimination of the complicated connection of the readout chip and the detector.

1.2 Introduction to SOI Monolithic Sensors

In this thesis, the author shows that one of the possible ways of the realization of a monolithic active pixel detector is exploitation of the SOI (Silicon On Insulator) technology based on the wafer-bonding process. Since a common SOI wafer consists of a thin layer of single-crystal silicon (device layer), separated from a bulk silicon substrate (support) by an electrically insulating layer [6], it is proposed to utilize the silicon support layer as the radiation sensitive substrate of the monolithic detector and to fabricate the readout electronics in a conventional way in the device layer.

Monolithic active pixel detectors realized in the SOI technology may have several important advantages. Like hybrid detectors, they allow efficient detection of ionising radiation in a fully depleted substrate, but they do not require any expensive assembling technology. As these sensors offer flexible choice of the readout scheme and the sensor thickness, they may find a wide range of applications - from medical diagnostics to particle physics experiments. These characteristics of the SOI monolithic sensors, along with continuously improving quality and lowering costs of wafer-bonded substrates encouraged the development of these devices.

The feasibility of the monolithic active pixel sensors in SOI technology was investigated in the past by different research teams (for example RD19 group from

CERN [7, 8]), but has never found successful implementation. The major difficulty in the realization of the monolithic sensors in the SOI technology is necessity of the development of dedicated, non-standard technology. For that reason, the author proposed and characterized a number of test structures, which allowed validation and parameters extraction of basic elements of the active sensors: transistors, detector junctions and modules of readout electronics. The developed technology allowed the author to design first prototypes of the new SOI detectors. Despite worse parameters of the detector junctions in comparison with the best modern hybrid sensors, functional sensors were manufactured. Performed tests showed their sensitivity to minimum ionising particles and low energy gamma radiation.

Author's research and development in the field of monolithic active pixel sensor is described in this thesis. After presentation of the principle of the operation of silicon pixel detectors and overview of existing solutions of these devices (chapters 2 and 3), the detailed description of the concept of the new SOI active pixel detector is given in chapter 4. Next, the discussion of the work on the sensor technology is performed in chapter 5. Finally, the architecture and the test results of the prototypes of the proposed SOI sensors are described in chapter 6.

1.3 Motivation

Although particle physics has been the main driving force for the development of advanced semiconductor detectors for last several decades, more and more often these devises enter new fields of applications. One of the areas of interests of physicists and engineers working on semiconductor detectors is medicine. The author's works on the monolithic active pixel detectors realized in SOI technology were motivated by medical applications of the SUCIMA ("Silicon Ultra-fast Cameras for Electron and Gamma Sources in Medical Applications") project[1], i.e. beam monitoring in hadrontherapy and radioactive sources dosimetry in brachytherapy [9].

Hadrontherapy is a successor of conventional radiotherapy, which is carried out with X-rays. It makes a use of proton beams (accelerated up to 200 MeV) or carbon ion beams accelerated up to 4700 MeV) for effective and selective tumour irradiation. Due to the well defined range of hadrons and the increase of the dose with the

[1]SUCIMA was a project supported by the European Commission within the Fifth Framework Program, carried on from 2001 to 2004

penetration depth, hadrontherapy is especially suitable for the treatment of deep-seated and located close to critical organs tumours [10, 11]. It has been reported that among the patients currently treated with conventional X-ray therapy, 30-40 % (i.e. 25000 patients per year in Europe) could benefit from the irradiation with light ion beams and the consecutive sub-sample of 10 % of those patients might have no better alternative of curing [12].

One of the problems related to the hadrontherapy is monitoring of the beam profile and intensity during the treatment. In existing hadrontherapy centres, there is no way to monitor on-line the beam parameters in the extraction lines and the beam quality is checked only by means of the dosimetric tools placed in front of the patient. For this reason, a new beam monitor, called SLIM (Sem for Low Interception Monitoring), has been proposed by the SUCIMA collaboration [13]. This tool was to allow on-line measurement of beam position, current and profile in the extraction lines of a hadrontherapy centre. The principle of operation of the SLIM monitor is illustrated in figure 1.2. The SLIM monitor bases on the collection of secondary electrons emitted at the passage of the beam through thin aluminium foils (0.2 - 0.4 micrometers thick). Such foils cause a negligible perturbation to the therapeutic beam. The liberated electrons are accelerated to 20 keV, focalized by appropriate optics and collected on a pixel detector. As the 20 keV electrons lose all their energy within several micrometers of silicon, the pixel detector should allow detection of short-range particles. One of the possible options is the SOI monolithic active pixel sensor with a shallow backplane contact.

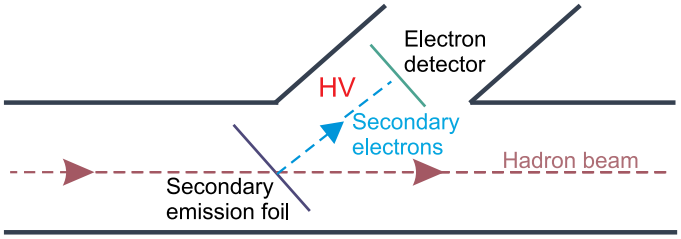


Figure 1.2: Current and profile measurements of hadron beam with SLIM [13].

Second application - intravascular brachytherapy is a post-angioplasty treatment of coronary artery disease. Coronary artery disease (CAD) is one of the main death causes in the United States and in Europe. It usually results from arteries narrowing and hardening due to cholesterol plaque build-up and leads to reduced blood flow to the

heart. One of the treatment methods of the coronary artery disease is angioplasty that relies on the re-establishing of the normal and stable artery cross section (lumen) by special balloons inflated at the blockage site in the artery [14, 15]. The main limitation of the angioplasty is the artery re-narrowing (restenosis), which affects about 40 % of the patients within 6 months from the intervention. Clinical studies show that the restenosis rate may drop from the original 30-40 % below 10 % if radiation is delivered to the obstruction site during or after angioplasty [16]. One of the methods of the dose (of 15 - 30 Gy) delivery to the re-narrowed vessel is intravascular brachytherapy. During the brachytherapy, the irradiation is usually selectively applied to a few centimetres long section of a vessel with the usage of the wire-shaped beta-emitting sources (e.g. ^{90}Sr/^{90}Y) with activities in the GBq range. The effectiveness of such a treatment is illustrated in figure 1.3.

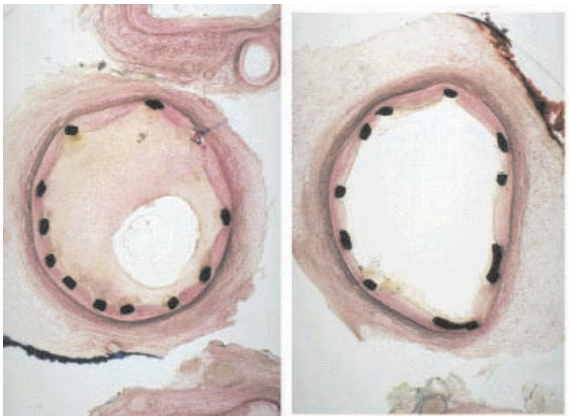


Figure 1.3: Cross sections of a vessel affected by the restenosis (left) and of a vessel for which the restenosis was reduced by brachytherapy treatment (right).

Safety of the brachytherapy requires precise quality control of the radioactive sources in hospitals. Defining an individual treatment plan for each patient involves also customisation of the sources basing on the analysis of the ultrasound images of the vessel. For that reason, SUCIMA collaboration proposed a real-time camera built of silicon detectors [17]. Apart of the real-time operation, the major benefit of such a tool is very good position resolution of the obtained images.

For the purpose of beam monitoring in hadrontherapy and radioactive sources dosimetry in brachytherapy, two competitive technologies of monolithic active pixel detectors were being developed within SUCIMA collaboration: CMOS and SOI [18].

At the beginning of the project, the CMOS solution was already well established. First prototypes had been qualified, signal-to-noise ratio up to 40 and microscopic resolution had been demonstrated [19, 20]. In turn, no earlier "know-how" existed for the SOI option. Therefore, the developments of the SOI detectors for the SUCIMA project were concentrated on basic feasibility study and the definition of novel sensor technology. It was expected that the new devices might be an attractive alternative for the CMOS monolithic active pixel sensors and hybrid detectors for SUCIMA and other imaging and tracking applications.

Chapter 2

Silicon Pixel Detectors - Principle of Operation

Monolithic active pixel detectors realized in silicon on insulator technology belong to a wide family of silicon detectors. Like in the conventional silicon detectors, the active volume of the SOI sensor is formed by a depleted region of a reverse biased p-n junction. When a particle traverses the active volume, it creates pairs of charge carriers. These charge carriers move under the influence of the applied external electric field and are collected on the contact electrodes. Such an induced signal is then processed by readout electronics connected to the detector electrodes.

Understanding of the concept of the SOI detector requires introduction to the basic physical phenomena underlying the principle of operation of silicon detectors. Such topics as properties of silicon as a detector material, the interaction of radiation with matter and the charge collection will be discussed in this chapter.

2.1 Silicon as Detector Material

Silicon is one of the most commonly used materials in semiconductor detectors. Great advantages of this material are established production techniques of high quality substrates and relatively well known properties. Since silicon is also basic material of integrated circuits, it offers the possibility of the integration of the detector and the readout electronics in one structure and allows achieving very good granularity.

Some important properties of silicon from the point of view of effective particles detection are summarized in table 2.1. Attractive features of silicon are its high density

and low energy required for the generation one electron-hole pair. The high density leads to a large energy loss per traversed length of ionising particle. This allows obtaining measurable signals even with the usage of thin detectors. Low energy for creation an electron-hole pair (an order lower than in gas detectors) ensures inherent good energy resolution and a large number of charge carriers generated by the detected particle. Despite the high density of silicon, the electron and hole mobilities for this material are still quite high which translates into relatively short collection times.

Table 2.1: Silicon properties at 300 K [21, 22].

Property	**Value**
Atomic number Z	14
Atomic mass A	28.0855
Density ρ [g cm^{-3}]	2.33
Band gap energy E_g [eV]	1.12
Energy per electron-hole pair E_{e-h} [eV]	3.6
Intrinsic carrier concentration n_i [cm^{-3}]	1.45×10^{10}
Electron mobility μ_e [cm^{2}V^{-1}s^{-1}]	1350
Hole mobility μ_h [cm^{2}V^{-1}s^{-1}]	450

Apart of silicon, some other materials are used for specific applications. For example gallium-arsenide and cadmium-telluride detectors are used in medical X-ray imaging and diamond detectors are planed to be used in harsh environment. Detection properties of these materials are, however, outside the topic of this thesis and will not be discussed.

2.2 Interaction of Radiation with Detector Material

The interaction of radiation with detector material that leads to the generation of measurable electric signal is a foundation of the particle detectors operation. The manner in which radiation interacts with the detector material depends on the nature of the incident particle and its kinetic energy, mass and charge. For simplicity, the consideration of the charge carries generation in the detector will be carried out separately for two types of particles – charged particles and photons.

2.2.1 Energy Loss by Heavy Charged Particles

When a charged particle traverses the detector material, it interacts with the electrons and the nuclei of atoms. Heavy charged particles lose their energy mainly in electromagnetic elastic collisions with shell electrons. If the energy transferred to the atomic electrons during such an interaction is large enough to extract them from the atom, the ionisation occurs. The mean rate of the ionisation energy loss for a moderately relativistic particle[1] is given by the Bethe-Bloch formula [21, 22]:

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2}\right) - \beta^2 - \frac{\delta}{2}\right] \tag{2.1}$$

where T_{max} is the maximum kinetic energy which can be imparted to a free electron in a single collision and $\frac{\delta}{2}$ is density effect correction. The other variables in formula 2.1 are defined in table 2.2.

Table 2.2: Summary of variables used in equations describing radiation interaction with detector material [21].

Symbol	**Definition**	**Value**	**Unit**
$\frac{dE}{dx}$	Energy loss	-	[eV $g^{-1}cm^2$]
K	$4\pi N_0 r_e^2 m_e c^2$	0.307	[MeV $g^{-1}cm^2$]
N_0	Avogadro's number	6.022×10^{23}	[mol^{-1}]
r_e	Classical electron radius	2.818×10^{-15}	[m]
m_ec^2	Electron mass $\times c^2$	0.510	[MeV]
c	Speed of light in vacuum	2.998×10^8	[m s^{-1}]
z	Charge of incident particle	-	-
Z	Atomic number of medium	14 for Si	-
A	Atomic mass of medium	28.0855 for Si	[g mol^{-1}]
β	Relative incident particle speed v/c	-	-
v	Incidebt particle speed	-	[m s^{-1}]
γ	Relativistic dilatation factor $1/\sqrt{1-\beta^2}$	-	-
I	Mean excitation energy	$\approx$ 172 for Si	[eV]
δ	Density effect correction	-	-
M	Incident particle mass	-	[MeV/c^2]

[1] Particle characterized by velocity larger than that of orbital electrons.

According to the Bethe-Bloch formula, the energy loss rate depends on the incident particle charge and only slightly depends on its mass due to expression describing T_{max}:

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma \frac{m_e}{M} + \left(\frac{m_e}{M}\right)^2} \tag{2.2}$$

The energy loss rate is also almost independent on the traversed media as the result of nearly constant Z/A ratio for most of the materials. The major parameter determining the energy loss rate is particle velocity.

The energy loss rate in silicon as a function of the $\beta\gamma$ factor calculated according to equation 2.1 is plotted in figure 2.1 (two upper curves). As illustrated, for slow, low energy particles, the energy loss rate decreases proportionally to $1/\beta^2$ and reaches broad minimum for $\beta\gamma \approx 3$. Particles having a mean ionisation energy loss rate in the region of this minimum (e.g. cosmic-ray muons) are called "minimum ionising particles" - MIPs. At higher particle velocities, the electric field surrounding the charged particle flattens and extends, and thus, the contribution of distant-collisions increases. This effect causes the logarithmic increase of the energy loss rate (relativistic rise). The logarithmic increase is limited by the polarization of the medium leading to the screening of the electrons in the more distant atoms. This effect is called density effect and its contribution to the mean energy loss rate, represented by $\frac{\delta}{2}$ in equation 2.1, is illustrated in figure 2.1.

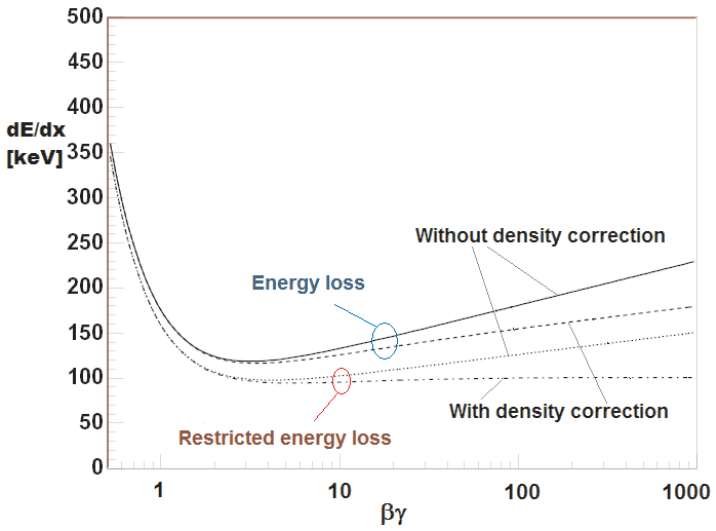


Figure 2.1: Energy loss rate and restricted energy loss rate as a function of $\beta\gamma$ for 300 μm thick silicon. The curves are plotted both with and without density correction [23].

The Bethe-Bloch formula (equation 2.1) describes the ionisation energy loss, while in practical detectors, the energy deposited along a particle track, rather than the energy lost, is measured. Some of the energy lost by a traversing particle may be carried of by energetic knock-on electrons (δ rays) and escape from the measurement. In such a case the mean energy loss excluding energy transfers greater than some cut-off energy T_{cut} should be considered. This leads to the following formula describing the restricted energy loss rate as the mean rate of the energy deposited along the particle track [21]:

$$-\left(\frac{dE}{dx}\right)_{restr} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_ec^2\beta^2\gamma^2T_{upper}}{I^2}\right) - \frac{\beta^2}{2}\left(1+\frac{T_{upper}}{T_{max}}\right) - \frac{\delta}{2}\right] \quad (2.3)$$

where $T_{upper} = \min(T_{cut}, T_{max})$.

The restricted energy loss rate calculated from above formula for $T_{cut} = 140$ keV is plotted in figure 2.1. One can see that for cut-off energies lower than T_{max}, T_{cut} replaces T_{max} in the argument of the logarithmic term of the formula 2.3 and the $\beta\gamma$ term producing the relativistic rise in the close-collision part of $\frac{dE}{dx}$ is replaced by a constant. Therefore, the ionisation energy loss rate approaches the constant "Fermi plateau".

The mean energy loss per unit absorber thickness (given by the Bethe-Bloch equation 2.1) does not describe the behaviour of a single particle traversing finite material thickness because of the stochastic nature of the energy losses. Since the number of collisions involving large energy transfers is very small (and most interactions involve little energy exchange), the single-collision spectrum is highly asymmetric. For this reason, the probability distribution function (pdf) $f(\Delta; \beta\gamma, x)$ describing the distribution of energy loss Δ in absorber thickness x (called straggling function) is also highly asymmetric. The pdf characterized by a long tail is usually called Landau distribution [24]. The Landau distribution is used for the experimental data fit and the extraction of the most probable energy loss in the detector. For the purpose of numerical calculations, the distribution is approximated by formula:

$$f(\lambda) = \frac{1}{\sqrt{2\pi}}\exp\left[-\frac{1}{2}\left(\lambda + \exp\left(-\lambda\right)\right)\right] \quad (2.4)$$

Where λ is a dimensionless parameter proportional to the energy loss:

$$\lambda = \frac{\Delta - \Delta_p}{\Delta_w}$$

Δ_p is the most probable energy loss and Δ_w is the width of the Landau distribution.

The formula 2.4 is known as the Moyal function [25] and is widly used for the detector calibration. It will be also exploited for the characterization of the SOI detectors in further chapters of this thesis.

Although the Landau distribution is the most commonly used description of the asymmetric energy loss distribution, it does not always agree with experimental results, especially for very thin layers. Examples of the distribution based on more recent calculations by Bichsel [26] are shown in figure 2.2. The distributions are plotted for different thickness values of the silicon material. As presented, with growing material thickness, the value of the most probable energy loss increases, approximately following the relation $x(a + \ln x)$. As the material thickness increases, the ratio of the most probably energy loss and the distribution width also increases. For very thick absorbers, where the energy loss exceeds one half of the original energy, $f(\Delta)$ begins to approximate a Gaussian distribution.

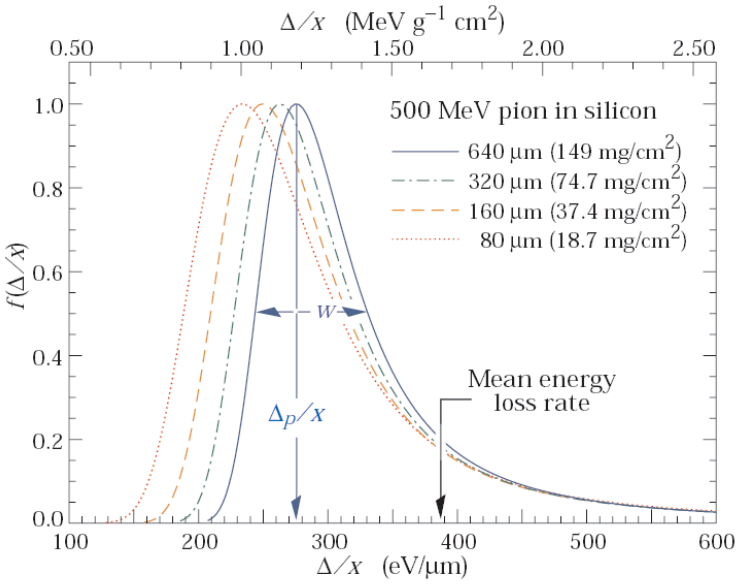


Figure 2.2: Distribution of energy loss in silicon for 500 MeV pions, normalized to unity at the most probable value $\Delta p/x$ [21].

The fluctuations in the deposited energy are significantly smaller than the fluctuations in the lost energy because energetic δ rays (responsible for the energy-loss tail to a large extend) can escape from the vicinity of the track. Therefore, the pdf describing the distribution of the restricted energy loss is characterized by less evident high energy tail.

2.2.2 Energy Loss by Electrons

The interactions of light charged particles, like electrons and positrons, with detector material differ from those discussed above for heavy particles. At low energies, electrons and positrons also lose energy primary by ionisation, but at high energies a bremsstrahlung process becomes dominant. The bremsstrahlung process originates from the interaction of the incident particle with the Coulomb field of the atomic nuclei and leads to the photon radiation. Different character of the ionisation energy loss of electrons and positrons results also from the identity of the incident electron with the atomic electrons which it ionizes [21]. For this reason, the Bethe-Bloch formula describing the energy loss rate by electrons and positrons has to be also modified taking into account the small mass of electrons. This modified formula assumes the maximum energy which is transferred during collision equal to half of the kinetic energy of the incident particle.

The contribution of the ionisation and bremsstrahlung loss rate to the total energy loss rate of a light particle traversing detector material depends on the energy of the particle. The ionisation loss rate rises logarithmically with energy, while the bremsstrahlung loss rate rises nearly linearly with energy. For this reason, at certain incoming particle energy E_c, the two loss rates are equal. This value of energy is called critical energy and, for solid materials, may be approximated by [27]:

$$E_c = \frac{610 \text{ MeV}}{Z + 1.24} \tag{2.5}$$

According to above formula, the critical energy E_c for silicon is of order of 40 MeV. It means that for the applications that motivated the development of the SOI detectors (beam monitor and brachytherapy source dosimetry), the ionisation energy loss is dominant and the bremsstrahlung is of minor importance.

2.2.3 Energy Loss by Photons

The manner in which photons interact with matter is fundamentally different from that of charged particles. When a photon traverses the detector active volume, it may loss energy or change direction through such processes like: photoelectric effect, Compton or Rayleigh (coherent) scattering and electron-positron pairs production. The probability of particular processes strongly depends on the incident photon energy E_γ. The photon absorption coefficients, which give probabilities of the particular process, as a function of the photon energy are presented in figure 2.3.

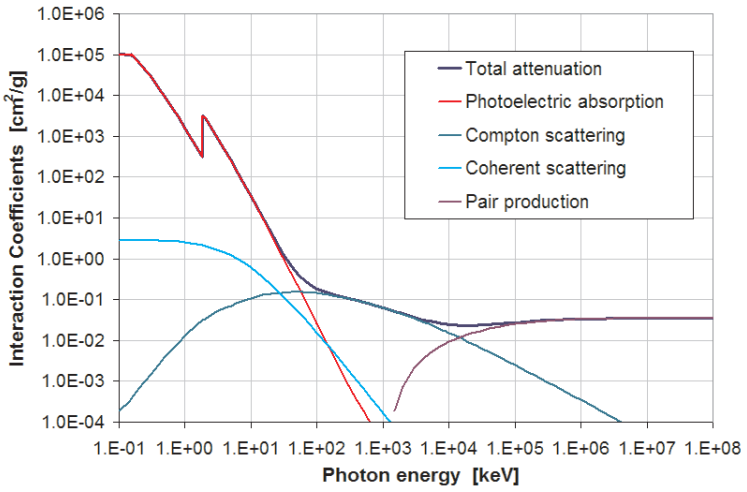


Figure 2.3: Photon interaction coefficients as a function of energy in silicon [28].

From the point of view of medical imaging applications (for example digital radiography) the main role plays interactions of low energy photons. For this energy range (for silicon up to several dozen keV), the dominating process is photoelectric effect, although Compton and Rayleigh scattering also contribute. The photoelectric effect relies on the absorption of a photon by an atomic electron followed by a subsequent ejection of the electron from atom. The absorption coefficient of this process is characterized by a discontinuity coming from the thresholds for photoionisation of various atomic levels. As the result of the photoelectric effect, the incoming photon disappears and the difference between the photon energy and the energy required for the extraction of the electron from atom is carried by the ejected electron. If the kinetic energy of the photoelectron is high enough, the electron may cause a secondary ionisation along its trajectory. If the photoelectron loses all its energy in the detector active volume, the number of electron-hole pairs created by ionisation corresponds to the energy of the incident photon. This phenomenon is often exploited for the calibration of the detector response.

The probability of the photoelectric effect decreases like $1/E_\gamma^{3.5}$ with the increasing photon energy and the Compton scattering becomes dominant in silicon detectors above 100 keV. The Compton scattering originates from elastic scattering of the incoming photon at a quasi-free atomic electron. During this interaction the photon changes direction and transfers part of its energy to the electron. In a given material, the probability of the Compton scattering is proportional to $\ln E_\gamma/E_\gamma$ [29].

As mentioned, another process that contributes at low energies is the Rayleigh scattering. In such an interaction no excess energy is transferred to the medium and no ionisation occurs. The photon continues traversing detector substrate, but its direction changes.

At energies higher than about 1.022 MeV, the process of photon conversion into an electron-positron pair in the Coulomb field of the nucleus may occur. This interaction is always accompanied by the atomic nucleus recoil, which allows fulfilling conservation of the energy and the momentum, simultaneously.

The contribution of a particular interaction for a given photon energy is of great importance for imaging applications. When a photon is absorbed by the photoelectric effect, the generated photoelectron deposits its energy in a very small, point like volume. Thus, very precise information about both the incident photon energy and the interaction position may be obtained. However, when any scattering occurs, the scattered photon may be absorbed at some distance from the primary photon trajectory. This results in degradation of the spatial resolution of the imaging system, and consequently, the deterioration of the image quality [30]. It is significant limitation of the use of silicon detectors in imaging applications.

2.2.4 Energy for Charge Carrier Generation in Silicon

The ionising energy loss of particles passing through detector leads to the creation of electron-hole (e-h) pairs in the detector active volume. The number of the generated charge carries N depends on the energy lost in the detector and the energy required for creation of an e-h pair in a given material. The interesting phenomenon is that the energy required for the creation of one electron-hole pair is always higher than the band gap energy E_g. This effect is ascribed to additional phonon excitation that is required for momentum conservation. In case of silicon, the mean energy that is necessary to generate an electron-hole pair is 3.62 eV. For the most probable energy deposition corresponding to a minimum ionising particle, it translates into the most probable number of charge carriers of about 22000 pairs in 300 μm thick detector.

Since both electronic and lattice excitations are involved in the energy deposition process, the number of the generated charge carriers for a given absorbed energy is a subject of random fluctuations. The variance in the number of generated charge carriers N is given by

$$\sigma_N^2 = FN \tag{2.6}$$

where F is Fano factor equal to approximately 0.1 for silicon [21]. Statistics in the process of the charge creation in the detector for events corresponding to the same energy release leads to the fluctuations of the measured signals in detecting systems. Nevertheless, these fluctuations are of minor importance in comparison with stochastic noise in readout electronics or energy loss fluctuations in the detector.

2.2.5 Multiple Coulomb Scattering

An important term related to the interaction of radiation with the detector material is multiple scattering. Introducing this term allows explaining the importance of the development of thin monolithic active pixel detectors for vertex detectors in high energy physics experiments.

A charged particle traversing a detector does not only lose its energy, but it is also deflected by many small-angle scatters. Most of these deflections are related to the Coulomb scattering from nuclei, and hence, the effect is called multiple Coulomb scattering. The angular scattering distribution of outgoing tracks for small deflection angles is almost Gaussian. For larger angles, which are more probable for low momentum particles than for high momentum ones, the distribution has larger tails than the Gaussian distribution. Nevertheless, for many applications, the angular scattering distribution may be approximated by the Gaussian distribution with the standard deviation described by formula [21]:

$$\theta_0 = \frac{13.6\ \text{MeV}}{\beta cp} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right] \tag{2.7}$$

where p, βc and z are momentum, velocity and charge number of the incident particle, respectively, and x/X_0 is the thickness of the scattering medium given in the quantity of radiation lengths[2].

The radiation length used in the above formula is a parameter that is characteristic of a given material and with accuracy better than 2.5% may be approximated by equation [21]:

$$X_0 = 716.4 \frac{\text{g}}{\text{cm}^2} \frac{A}{Z(Z+1)\ln(287/\sqrt{Z})} \tag{2.8}$$

[2]Radiation length is a mean distance over which a high-energy electron loses all but $1/e$ of its energy by bremsstrahlung and it is 7/9 of the mean free path for pair production by a high-energy photon [21].

The radiation length for silicon is $X_0 = 21.82$ g/cm^2. Sometimes the radiation length is also normalized to the material density, and then the value of 9.36 cm is given for this material [21].

For vertex detectors in high energy physics experiments, the multiple scattering may result in significant reduction of the measurement precision. The performance of any pixel-based vertex detector can be expressed by the precision of the measurement of the track impact parameter, which is defined as the closest approach of the reconstructed track to the primary vertex or the beam-spot of collision. The impact parameter resolution of a vertex detector is a convolution of the point measurement precision, mechanical stability and multiple scattering effects [31]. Since, according to formula 2.7, the thicker is the medium the larger is the deflection of the particle trajectory, very thin pixel detectors are required in order avoid multiple scattering in the vertex detector layers. It can be achieved by development of thin monolithic active pixel detectors, which do not require separate structures for readout electronics and can be thinned down to several dozens of micrometers.

2.3 Silicon Detector as a p-n Junction

The previous sections described the interaction of the particles with matter and the mechanism of the charge carries generation in the detector volume. One might notice that the most probably charge generated by a MIP particle in 300 μm thick silicon is about 2.2×10^4, while, even in pure silicon, the intrinsic carrier density is $n_i = 1.45 \times 10^{10}/\text{cm}^3$, which translates into the total number of free carries of 4.35×10^8 for a the detector with the same thickness and surface of 1 cm^2. Thus, to be able to measure typical signals generated by particles, the free carriers should be removed from the detector active volume. In practical applications, it is achieved by the usage of the reverse biased p-n junction. Space charge region of such a junction forms the detector sensitive volume.

2.3.1 Evaluation of Sensitive Region Thickness

The thickness of the detector active region may be calculate relying on the Poisson equation and the condition of the crystal neutrality. Assuming that the junction has the form of an abrupt junction (illustrated in figure 2.4) and the p and n regions have the impurities concentrations of N_A and N_D, respectively, the neutrality condition is

given by:

$$qN_AW_p = qN_DW_n \tag{2.9}$$

where W_p and W_n are widths of the depletion layers on the p and n sides of the junction and q is an elementary charge.

One-dimensional Poisson equation for the structure depicted in figure 2.4 has the following form:

$$\frac{d^2V}{dx^2} = -\frac{\rho_d}{\varepsilon_{Si}\varepsilon_0} = \begin{cases} \frac{qN_A}{\varepsilon_{Si}\varepsilon_0} & \text{for} \quad -W_p \leq x \leq 0 \\ -\frac{qN_D}{\varepsilon_{Si}\varepsilon_0} & \text{for} \quad 0 \leq x \leq W_n \end{cases} \tag{2.10}$$

where ρ_d is the charge density in the depleted region, ε_0 is permittivity of free space and ε_{Si}=11.9 [21] is silicon dielectric constant. The equation describing electric field $E(x)$ is derived after the integration of above formula with the boundary conditions of $E(-W_p) = E(W_n) = 0$. One obtains:

$$E(x) = \begin{cases} -\frac{qN_A}{\varepsilon_{Si}\varepsilon_0}(x + W_p) & \text{for} \quad -W_p \leq x \leq 0 \\ \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(x - W_n) & \text{for} \quad 0 \leq x \leq W_n \end{cases} \tag{2.11}$$

Second integration of the formula 2.10 with the boundary conditions of $V(-W_p) = 0$ and $V(W_n) = V$ leads to the following distribution of the electrostatic potential $V(x)$:

$$V(x) = \begin{cases} \frac{qN_A}{2\varepsilon_{Si}\varepsilon_0}(x + W_p)^2 & \text{for} \quad -W_p \leq x \leq 0 \\ -\frac{qN_D}{2\varepsilon_{Si}\varepsilon_0}(x - W_n)^2 + V & \text{for} \quad 0 \leq x \leq W_n \end{cases} \tag{2.12}$$

Obtained distributions of the electric field and the electrostatic potential in the discussed abrupt p-n junction are presented in figures 2.4-c and 2.4-d.

Equation 2.12 allows calculation of the potential barriers V_p and V_n in the p-type and n-type layers respectively:

$$V_p = \frac{qN_AW_p^2}{2\varepsilon_{Si}\varepsilon_0} \tag{2.13}$$

$$V_n = \frac{qN_DW_n^2}{2\varepsilon_{Si}\varepsilon_0} \tag{2.14}$$

The sum of above potential barriers is equal to the total potential difference at the junction. Therefore:

$$V_{bi} + V_{DET} = V_p + V_n = \frac{q}{2\varepsilon_{Si}\varepsilon_0}(N_AW_p^2 + N_DW_n^2) \tag{2.15}$$

where

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_AN_D}{n_i^2}\right)$$

is "built in" voltage of the junction and V_{DET} is external reverse bias voltage. Putting the neutrality condition 2.9 into equation 2.15, the following formula expressing the

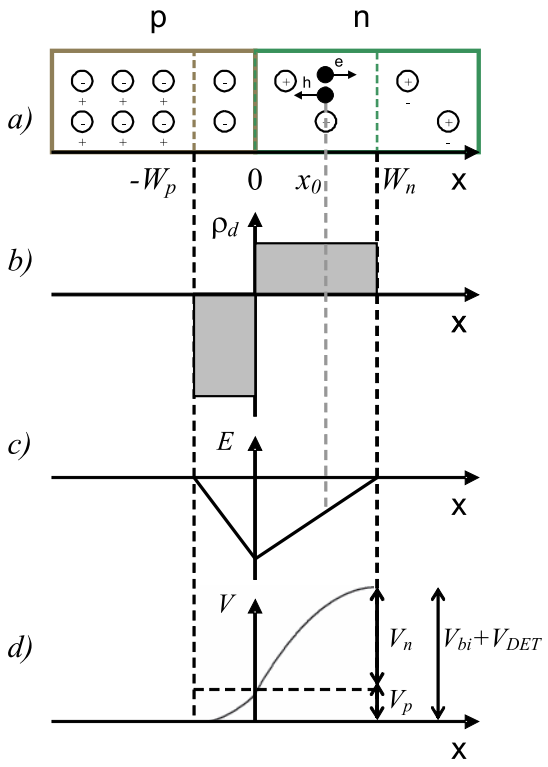


Figure 2.4: A p-n junction: a) cross-section with marked position and motion of generated e-h pair, b) space charge density, c) electric field distribution and d) electrostatic potential distribution.

total thickness W_d of the depleted region as a function of the potential difference at the junction is obtained:

$$W_d = W_p + W_n = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0(V_{bi} + V_{DET})(N_D + N_A)}{qN_D N_A}} \tag{2.16}$$

Detectors typically use an asymmetric structure, e.g. a highly doped p electrode and a lightly doped n region, so that the depletion region extends predominantly into the lightly doped volume. In the case of the SOI detector, the $p^+ - n$ detector structure is used. The thickness of the depleted region for such a detector may be approximated by:

$$W_d \approx \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0(V_{bi} + V_{DET})}{qN_D}} \tag{2.17}$$

Above equation is often used for the evaluation of the full depletion voltage, i.e. the external voltage at which the total thickness of the detector becomes depleted.

The formula describing the relation between the thickness of the sensitive region and the impurities concentration in the detector material has an important consequences on the choice of the detector material. One can see that, according to equation 2.17, lightly doped detector substrates should be used in order to avoid biasing the detector with very high voltages. Thus, the typical values of the impurities concentrations in the detector materials are of order of 10^{11}cm^{-3} - 10^{12}cm^{-3}.

2.3.2 Leakage Current and Junction Capacitance

The most important parameters of the p-n junction working as a radiation detector are leakage current and junction capacitance. These parameters significantly affect the signal-to-noise ratio of detecting systems. The shot noise related to the detector leakage current always contributes to the total noise of the sensor. As it will presented later, in the case of the monolithic active pixel detector realized in SOI technology, the leakage current may also lead to the saturation of the readout electronics due to the DC coupling of the collecting junctions with the processing circuit. Moreover, the junction capacitance is an important factor for calculation of the charge-to-voltage conversion gain of the SOI detector. Thus, the measurements of the current versus voltage (I-V) and capacitance versus voltage (C-V) characteristics of the detector belong to the basic set of the detector tests. They allow evaluation of the detector quality and determination of the full depletion voltage.

The leakage current originates from the thermal generation of electron-hole pairs in the detector material. The leakage current has to components: the generation current and the diffusion current. The generation current is the result of the generation process in the depletion region of the detector. In this region, the generated charge carries are separated by electric field, and hence, practically cannot recombine. They drift under the influence of the electric field and give the rise to the leakage current. The density of the generation current is expressed by [32]:

$$j_{gen} = \frac{q n_i W_d}{\tau_g} \tag{2.18}$$

where τ_g is generation lifetime.

The generation current density depends on substrate quality, temperature and applied external voltage. The substrate quality determines the generation lifetime τ_g, which is a function of the trap density N_t, the trap energy levels E_t in the band gap

and the electron σ_n and hole σ_p capture cross-sections. For a simplified case of a single trap level and equal electron and hole capture cross-sections σ_n=σ_p=σ_0, the generation lifetime is given by:

$$\tau_g = \frac{2\cosh\left(\frac{E_t - E_i}{kT}\right)}{\sigma_0 \nu_{th} N_t} \tag{2.19}$$

where ν_{th} is thermal velocity and E_i is intrinsic energy level. This simplified formula shows that especially the trapping centres with energy levels close to the midgap may significantly affect the generation lifetime and the detector leakage current.

The temperature dependence of the generation current density derives from the dependence of the intrinsic carrier concentration n_i and the generation lifetime τ_g on the temperature. Since the intrinsic carrier concentration increases by factor of two with temperature increase of 8 degrees, the detector should operate at low and constant temperature in order to achieve low and stable leakage currents.

At last, according to formulas 2.17 and 2.18, the generation current density depends on the reverse bias voltage. The generation current for a good detector should increase linearly with $\sqrt{V_{DET}}$ until reaching full depletion, and then it should stay constant.

Apart of the generation current, the diffusion current that is related to the generation process in undepleted regions may also contribute to the leakage current. It occurs when e-h pairs are generated close to the space charge region and have a chance to diffuse into it before recombination. Denoting by τ_n and τ_p the lifetime of electrons in the p-type region and the lifetime of holes in the n-type region, respectively, the widths of the layers from which the carriers may reach the depletion zone (diffusion lengths) are equal $L_n = \sqrt{D_n \tau_n}$ and $L_p = \sqrt{D_p \tau_p}$, where D_n and D_p are electron and holes diffusion constants. The diffusion current density is approximated by [33]:

$$j_{diff} \approx q n_i^2 \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} \right) \tag{2.20}$$

which for an asymmetric junction characterized by $N_A \gg N_D$ amounts to:

$$j_{diff} \approx q \frac{n_i^2}{N_D} \sqrt{\frac{D_p}{\tau_p}} \tag{2.21}$$

In general, the leakage current is a sum of generation current and diffusion current. Under normal operating condition, many silicon detectors (including SOI detectors) are fully depleted and the leakage current is determined by the generation current defined by equation 2.18.

As mentioned, another important parameter of a silicon detector is the junction capacitance. This parameter is defined by the charge increment dQ (on either side of the junction) resulting from the applied voltage increment dV_{DET}:

$$C_j = \frac{dQ}{dV_{DET}} = \frac{dQ}{dW_d}\frac{dW_d}{dV_{DET}} \tag{2.22}$$

Taking into account equations 2.9 and 2.17 one obtains:

$$C_j = \sqrt{\frac{q\varepsilon_{Si}\varepsilon_0 N_D}{2(V_{bi} + V_{DET})}} \tag{2.23}$$

The junction capacitance decreases with increasing bias voltage until the whole detector thickness is depleted. Since that moment, the capacitance becomes constant because further voltage increase does not change the charge. This effect is often exploited for the extraction of the full depletion voltage from C-V characteristics.

2.4 Configurations of Segmented Detectors

In practical applications, one or both electrodes of the p-n junction of a detector are segmented, creating one or two-dimensional arrays of detection systems. Such a configuration allows obtaining the information about the position at which the particle passed through the detector. As illustrated in figure 2.5, depending on the shape of the detector segments, strip or pixel detectors may be distinguished.

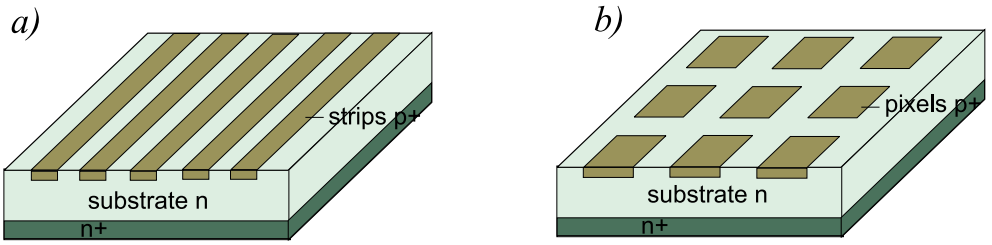


Figure 2.5: Configurations of segmented detectors: a) strip detector, b) pixel detector.

Strip detectors are the simplest configuration of segmented detectors. They have mostly found an application in high precision tracking in high energy physics experiments [33, 34, 35]. Strip detectors are usually built of several centimetres long, parallel strip-like p^+ implants on a lightly doped n-type substrate. Sometimes n^+ strips

(perpendicular to the p^+ strips) are also created on the n-side of the junction in order to obtain two-dimensional information about particle track position. Such a structure is called double-sided strip detector. The double-sided detectors have several drawbacks. First of all, the positive charge trapped at the silicon-silicon dioxide interface may result in accumulation of electrons between the n^+ strips and cause short circuit of the electrodes. One of the methods that allow to overcome this problem is the implantation of the p-type channel stoppers between the particular strips on the n^+ side of the detector. The double-sided detectors have also limited use in the applications in which high particle fluxes are expected. If multiple particles are passing the detector, the positions of the particular trajectories might not be reconstructed unambiguously.

More advanced detector configuration, which allows two-dimensional particle trajectory reconstruction, is a pixel detector. The pixel detector have a form of an array of p-n diodes created on a common high resistivity substrate. Typical distance between the centers of adjacent pixels (so called "pitch") is of order of few tens or few hundreds of micrometers, which allows achieving good spatial resolution. Such detectors have a wide range of applications – from high energy physics experiments to medicine [36, 37, 38].

An intermediate configuration between the strip and pixel detector is pad detector, which also consists of a matrix p^+ segments, but the size of the segments is of order of a few dozen of square millimetres. One of the applications of the pad detectors is energy spectroscopy [22].

The electrodes of described above segmented detectors are usually connected to an integrated circuit, called front-end or readout chip, which provides first signal amplification and filtering. The system built of a radiation sensitive detector and associated readout electronics is called active detector. The methods of the integration of the segmented detector with the front-end electronics are different for the strip and pixel detectors. The front-end chip for strip and pad detectors is located at the edge of the detector and it is connected with particular strips or pads by wire-bonding technique. The front-end electronics for pixel detectors has a form of two-dimensional matrix and its particular channels are placed in the same or separate silicon structure in the direct vicinity of the corresponding pixel. The methods of the integration of the pixel detectors with their readout electronics for existing solutions of the pixel detectors and the SOI detector will be presented in next chapters.

2.5 Signal Formation on Detector Electrodes

As presented in previous sections, the active volume of a silicon detector is formed by the depleted region of p-n junction. If charge carries are generated inside this active region as the result of ionising energy loss, they drift towards detector electrodes. This charge carriers motion induces a current signal on the detector electrodes, which can be measured and processed by readout electronics. The induced current signals for a planar p-n junction or a detector with segmented electrodes (pixel or strip detector) may be evaluated using the Ramo's theorem [39]. Using this method, the induced current on the particular electrode can be calculated relying on the "weighting field" $\vec{E}_w$ that describes the electrostatic coupling between the moving charge and the sensing electrode. The weighting field is determined by applying unit potential to a selected sensing electrode and grounding other electrodes. It depends on the detector geometry and has to be determined for every electrode for which the signal is to be resolved. In the most general form, the current induced on m^{th} electrode by a moving charge q is given by [40]:

$$i_m(t) = -q\vec{E}_w(P(t)) \cdot \vec{\nu}(P(t)) = q\vec{\nabla}\Phi_w(P(t)) \cdot \vec{\nu}(P(t)) \tag{2.24}$$

where $\vec{E}_w(P)$, $\Phi_w(P)$ and $\vec{\nu}(P)$ are respectively weighting field, weighting potential and velocity of the charge carrier at the position P. This equation describes the partial contribution to the induced current at time t that arises from an elementary bunch of charge q of the initial ionisation track. The actual shape of the induced current may be computed by summing up all the elementary contributions into which the initial track can be split [41].

The velocity of the charge carrier may be obtained from the drift motion low:

$$\vec{\nu}(P) = \mu\vec{E}(P) \tag{2.25}$$

where μ is mobility of the charge carrier and $\vec{E}(P)$ is electric field at position P. At room temperature (300 K), this formula is valid up to electrical fields of 10^4 V/cm, when the charge velocity is proportional to the electric field. For this operation regime, the electron and hole mobilities are constant and equal to μ_e=1350 cm^2/Vs and μ_h=450 cm^2/Vs, respectively.

Determination of the weighting field is more complex task. In general, the weighting field is different than the distribution of the physical electric field at the operating conditions. In the case of strip or pixel detectors, the weighting field is usually strongly

peaked near the sensing electrode, and thus, most of the signal is induced when the charge carrier approaches the electrode. Exemplary shapes of the weighting potential lines and corresponding current signals for the sensing electrode of a segmented detector are presented in figure 2.6. As presented, the values of the induced current follow the weighting potential gradient $\vec{\nabla}\Phi_w(P(t)) = \vec{E}_w(P(t))$ at the particular position in the detector volume. If the charge carrier is not generated directly under the sensing electrode (examples "b" and "c"), the current changes sign as the carrier moves in the physical electric field. In the extreme case when the charge carrier is not collected on the selected sensing electrode, the induced current changes in such a way that the integrated signal value (integrated charge) is equal to 0.

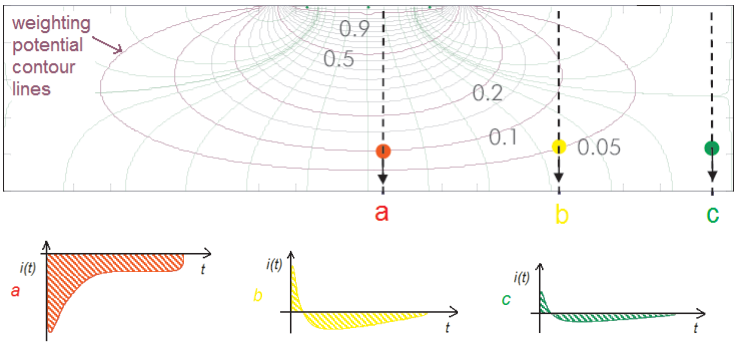


Figure 2.6: Weighting potential and induced currents for a segmented detector [42].

The analysis of the induced currents simplifies for detectors with planar (two-electrode) geometry. Assuming that the detector has a form of an asymmetric $p^+ - n$ junction, the weighting field is constant and equal to $1/W_d$, where $W_d \approx W_n$ is thickness of the depletion region expressed by 2.17.

The electric field distribution that is required for the evaluation of the velocity of the charge carriers for fully depleted planar detector is given by equation 2.11. If the detector is over depleted – the bias voltage is higher than the full depletion voltage – the absolute value of the electric field inside the detector is increased by $E_{min} > 0$ and the electric field on the n-type side of the junction is given by:

$$E(x) = \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(x - W_d) - E_{min} \tag{2.26}$$

Assuming that at the time $t = 0$ an electron-hole pair is created at the position x_0 such as $0 \geq x_0 \geq W_d$ (figure 2.4), the following motion equations for the charge

carriers may be obtained by putting formula 2.26 into the motion low 2.25:

$$\frac{ds}{dt} = \mu_h \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} s + \mu_h E_{min} \Bigg|_{s=W-x} \quad \text{for the hole} \tag{2.27}$$

$$\frac{ds}{dt} = -\mu_e \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} s - \mu_e E_{min} \Bigg|_{s=W-x} \quad \text{for the electron} \tag{2.28}$$

Integrating above equations with the initial conditions $x = x_0$ at $t = 0$, the following time dependencies of the hole and electron positions are computed:

$$W_d - x_h(t) = -\frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min} + \left(W_d - x_0 + \frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min} \right) \exp\left(\mu_h \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) \tag{2.29}$$

$$W_d - x_e(t) = -\frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min} + \left(W_d - x_0 + \frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min} \right) \exp\left(-\mu_e \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) \tag{2.30}$$

This leads to the time dependencies of the hole and electron velocities described by equations:

$$\nu_h(t) = -\mu_h \left[\frac{qN_D}{\varepsilon_{Si}\varepsilon_0} (W_d - x_0) + E_{min} \right] \exp\left(\mu_h \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) \tag{2.31}$$

$$\nu_e(t) = \mu_e \left[\frac{qN_D}{\varepsilon_{Si}\varepsilon_0} (W_d - x_0) + E_{min} \right] \exp\left(-\mu_e \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) \tag{2.32}$$

Once the weighting field and carriers velocities are known, the currents induced on the detector cathode by the hole and electron motions are obtained in the following forms:

$$i_h(t) = \begin{cases} \frac{q}{W_d}\mu_h \left[E_{min} + \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(W_d - x_0) \right] \exp\left(\mu_h \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) & \text{for} \quad 0 \le t \le t_h \\ 0 & \text{for} \quad t > t_h \end{cases} \tag{2.33}$$

$$i_e(t) = \begin{cases} \frac{q}{W_d}\mu_e \left[E_{min} + \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(W_d - x_0) \right] \exp\left(-\mu_e \frac{qN_D}{\varepsilon_{Si}\varepsilon_0} t \right) & \text{for} \quad 0 \le t \le t_e \\ 0 & \text{for} \quad t > t_e \end{cases} \tag{2.34}$$

where t_h and t_e are collections times of the hole and the electron, respectively. Since $x_h = 0$ for $t = t_h$ and $x_e = W_d$ for $t = t_e$, the collection times can be derived from equations 2.29 and 2.30 in the following forms:

$$t_h = \frac{\varepsilon_{Si}\varepsilon_0}{\mu_h q N_D} \ln \frac{W_d + \frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min}}{W_d - x_0 + \frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min}} \tag{2.35}$$

$$t_e = \frac{\varepsilon_{Si}\varepsilon_0}{\mu_e q N_D} \ln \frac{W_d - x_0 + \frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min}}{\frac{\varepsilon_{Si}\varepsilon_0}{qN_D} E_{min}} \tag{2.36}$$

Time integration of equations 2.33 and 2.34 allows also calculating the charge induced by a hole and an electron on the cathode as a function of time:

$$Q_h(t) = \int_0^t i_h(t)dt = \frac{\varepsilon_{Si}\varepsilon_0}{W_d N_D}\left[E_{min} + \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(W_d - x_0)\right]\left[\exp\left(\mu_h \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}t\right) - 1\right] \quad (2.37)$$

$$Q_e(t) = \int_0^t i_e(t)dt = \frac{\varepsilon_{Si}\varepsilon_0}{W_d N_D}\left[E_{min} + \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}(W_d - x_0)\right]\left[1 - \exp\left(-\mu_e \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}t\right)\right] \quad (2.38)$$

Finally, the total contributions of the electron and hole motions to the total charge induced on the detector cathode may be obtained by introducing the hole and electron charge collection times (t_h and t_e) into the above formulas:

$$Q_{h,tot} = q\frac{x_0}{W_d} \quad (2.39)$$

$$Q_{e,tot} = q\frac{W_d - x_0}{W_d} \quad (2.40)$$

Some exemplary theoretical shapes of the current signals obtained for different values of E_{min} and different positions x_0 of the creation of the electron-hole pair in the detector are illustrated in figure 2.7. The presented results were calculated using parameters typical for SOI detectors: $N_D = 5\times10^{11}/\mathrm{cm}^3$ and $W_d = 400\ \mu$m and relying on equations 2.33, 2.34, 2.35 and 2.36. The illustrated current signals were obtained under assumption of a planar detector geometry and may differ from those induced in segmented detectors. Nevertheless, they show the general dependence of the pair generation position and detector bias on the shape of the signal formed on the detector electrodes. One can see that over-depleting of the detector allows reducing the charge collection times.

The discussion of the signal formation in the silicon detectors was performed neglecting the charge carriers diffusion and trapping. In practical cases, the diffusion causes the charge spread along the particle track, while trapping causes the reduction of the amount of the drifting charge. The importance of both of this effects depends on the drift time. The average square deviation σ^2_{diff} of the charge transverse distribution after the collection time is given by [41]:

$$\sigma^2_{diff} = 2D_{n,p}\ t_{e,h} \quad (2.41)$$

Although the diffusion coefficient is smaller for holes, the width of the charge cloud coming to the surface of the detector is usually similar for electrons and holes due to unequal charge collection times of both carriers.

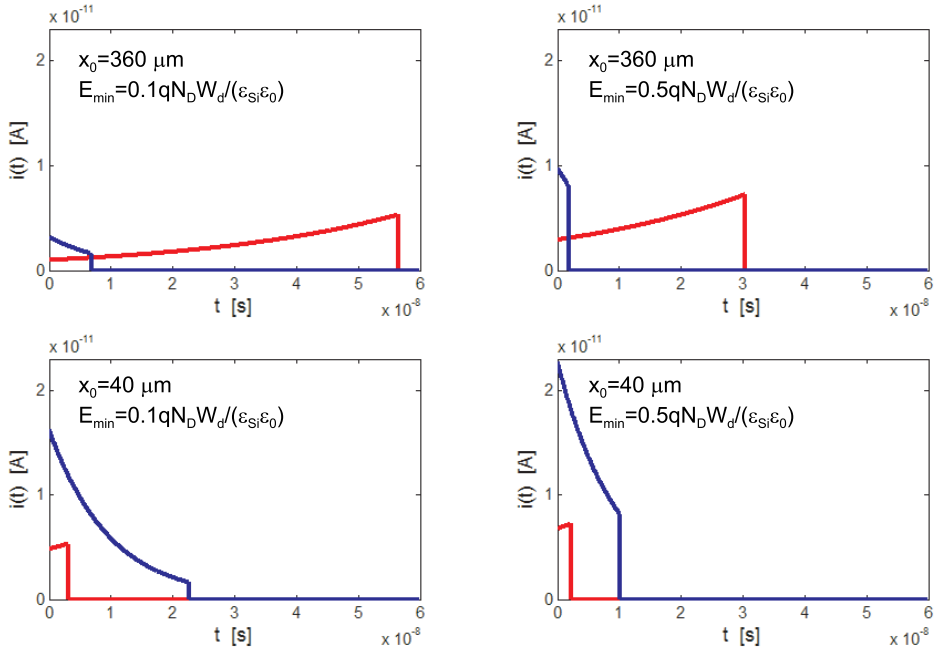


Figure 2.7: Examples of current signals induced on the cathode of 400 μm thick planar detector by the motion of a electron-hole pair. Red and blue lines indicate signals induced by the hole and electron motions, respectively.

The charge trapping is usually included in calculations of the current and charge signals induced on the detector electrodes by modifying formula 2.24 in the following way:

$$i_m(t) = -q \exp\left(-\frac{t}{\tau_{eff}}\right) \vec{E}_w(P(t)) \cdot \vec{\nu}(P(t)) \tag{2.42}$$

where τ_{eff} is effective carrier trapping time. The importance of the charge trapping increases significantly for radiation damaged detectors, in which the effective trapping times may become comparable with the charge collection times [43].

Chapter 3

Existing Solutions of Silicon Pixel Detectors

The basic structure of a pixel detector that was presented in previous section has been constantly improved leading to the construction of several competitive solutions of active pixel detectors. The existing solutions of silicon pixel detectors may be in principle divided into two subgroups – hybrid detectors and monolithic detectors. In the hybrid detectors, the radiation sensitive part and the front-end chip are separate entities, while in the monolithic detectors, both parts of the active sensor are integrated in one structure.

The knowledge of the available solutions of the pixel detectors is necessary for understanding the motivation for the development of monolithic active pixel detectors realized in silicon on insulator technology. For this reason, the major achievements in the field of both hybrid and pixel detectors will be discussed in the following sections.

3.1 Hybrid Active Pixel Detectors

Hybrid active pixel detectors are the most classical, but also the most mature kind of pixel detectors. The charge collection in these detectors is conventional and relies on the charge generation and transport in the fully depleted space charge region of a p-n junction. As mentioned, in the case of the hybrid detectors, the readout electronics and the detector sensitive volume are processed independently. Both parts of the detector are connected together by flip-chip bonding technique and form a "sandwich-like" structure presented in figure 3.1-a. Such an approach allows optimizing substrate

parameters and manufacturing process for both the sensitive pixel matrix and the front-end electronics. The sensitive part is usually manufactured on a high resistivity silicon substrate with the typical thickness ranging from 100 μm to 500 μm, but other detector materials, like GaAs or diamond, can be also exploited. The readout electronics is manufactured on a low resistivity silicon substrate using standard or radiation hard CMOS or BiCMOS processes. The recent reports showing good radiation hardness of modern commercial deep-submicron CMOS technologies [44, 45] open the way for the development of relatively cheap, more functional and higher granularity readout electronics for the hybrid detectors.

A great challenge in the development of hybrid detectors is still establishment of the electrical connection between the front-end chip and the sensitive pixel matrix. This is performed by a complex and expensive bump-bonding flip-chip process, which involves several steps: deposition of bonding pads on the detector and the front-end chip, bump formation, flip-chip alignment and placing, annealing or adhesive bonding [46]. The conductive bumps used in the bump-bonding process have typically the shape of small solder or indium balls, formed on under-bump metallization made of gold or other metal. A microscope photography of the indium bumps applied on a read-out chip is presented in figure 3.1-b.

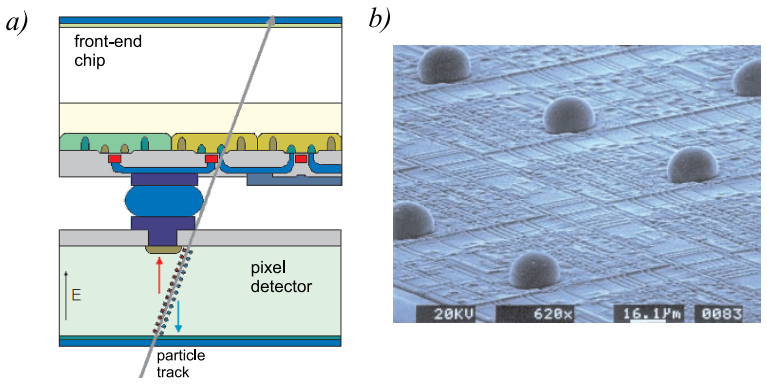


Figure 3.1: a) Cross-section of a hybrid active pixel detector [47]. b) Scanning electron microscope photography of the indium bumps applied on read-out chip. [48].

Nowadays, depending on the applied bump-bonding technique, the minimum bump pitch ranges from 20 μm to 250 μm. The minimum distance and the size of the bumps, together with the minimum area required for a single channel of the readout electronics are the main limiting factors for achieving good spatial resolution of the hybrid pixel detectors. Typical single cell dimensions of the present hybrid detectors are of order

150 μm x 150 μm (pixel detector for CMS experiment) or 50 μm x 400 μm (detector for ATLAS experiment) [5]. To overcome this limitation, a detector configuration with interleaved pixel implants between readout nodes has been proposed [49]. The layout of the pixel detector with interleaved pixels is illustrated in figure 3.2. In the presented configuration, the charge generated underneath one of the interleaved pixels induces a signal on the capacitively coupled read-out pixels. This leads to a spatial accuracy improvement by a proper signal interpolation. The experimental results have shown that the spatial resolution of 3 μm and the charge loss below 40 % may be achieved using interleaved pixel detectors [50].

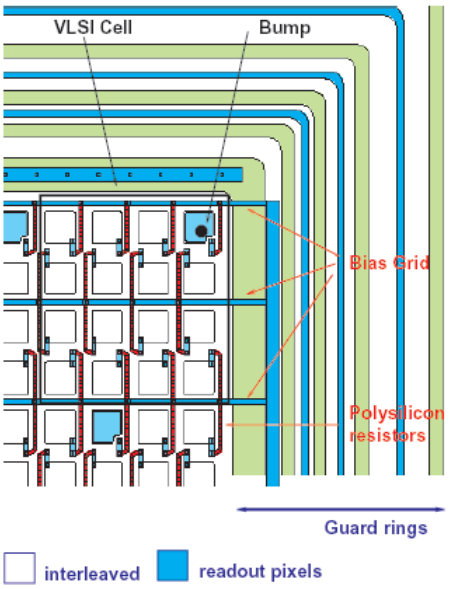


Figure 3.2: Layout of an interleaved pixel detector. Structure with 50 μm implant pitch and 200 μm read-out pitch [49].

Although the hybrid pixel detectors have many attractive features, a serious disadvantage of these detectors is their total thickness. Typically, in order to obtain mechanical stability, the required thickness of the sensitive pixel matrix and the readout chip are 100 μm and 50 μm, respectively. This makes these sensors unsuitable for future high energy physics experiments, which usually require maximum total active sensor thickness $\leq$ 50 μm . For this reason, a smaller interest in the development of silicon hybrid detectors may be recently observed. However, it may be expected that these detectors as an efficient, reliable and well established solution will still play crucial role both in experimental physics and medical applications.

3.2 Monolithic Active Pixel Detectors

Monolithic active pixel detectors are alternative solutions of active pixel detectors that currently arouse special interest. It is expected that the monolithic approach will not only enable reducing material budget in future particle physics experiments, but will also allow lowering the cost of the detector assembling due to the elimination of the complicated bump-bonding flip-chip process. Despite many attractive features, the monolithic pixel detectors have several drawbacks. Their parameters cannot be usually as efficiently optimized as in the case of the hybrid detectors and their operation principle often involves physical effects that are not considered in hybrid detectors.

At present, a dynamic development in the field of monolithic active pixel detectors may be observed. Some of proposed monolithic detectors exploit commercially available technologies, while the others require the development of non-standard, complex processes. As the examples of both approaches, the CMOS and DEPFET sensors will be reported in the following sections. A more extensive overview of the monolithic detector technologies may be found in [5].

3.2.1 CMOS Detectors

On the contrary to other monolithic detectors, the CMOS monolithic active pixel sensors (CMOS MAPS) are produced in commercially available twin-well CMOS technologies. It translates into lower manufacturing costs of these sensors, but also into the necessity of following the changes on the microelectronics technology market.

The concept of the CMOS monolithic active pixel detectors was derived from visible light sensors. The cross-section of the device is illustrated in figure 3.3. Unlike the conventional hybrid detectors, the CMOS devices operate only at partial depletion. The active volume of the CMOS detector is constituted by a lightly doped epitaxial layer, in which electron-hole pairs are created by traversing particles. The generated electrons thermally diffuse towards the potential minima located at the collection n-wells. Because of the large difference of doping levels between the p-epitaxial layer and the p-wells and substrate, potential barriers are created at the active region boundaries. This allows collection of almost all the generated electrons only by the sensing n-wells.

As the n-well/p-epi diode forms the sensitive element, the readout electronics in CMOS detectors can be only implemented in the p-wells, and thus, it may only use

NMOS transistors[1]. This limits the flexibility of the design of the front-end electronics. The typical structure of the readout channel for the CMOS sensor is presented in figure 3.3-b. This configuration is called three transistor (3T) cell and is composed of the input source follower transistor, the reset transistor that discharges the charge-integrating input capacitance and the switch connecting the selected cell to the output line. Recently, novel configurations of the readout channels allowing correlated double sampling processing directly in the pixel cell have been also reported [52, 53].

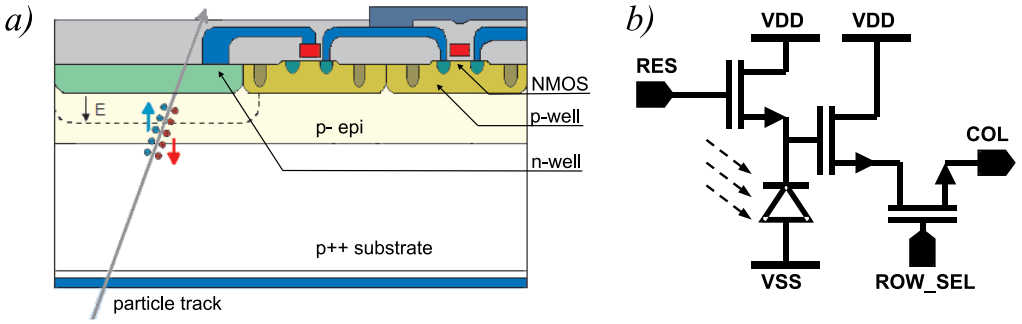


Figure 3.3: a) Cross-section and b) basic configuration of a readout cell of CMOS monolithic active pixel detector.

Since the CMOS active pixel detectors may be manufactured in modern deep-submicron technologies, they allow achieving readout pitch below 20 μm and spatial resolution of 1.5 μm [54]. The price to be paid is small thickness of the active volume, which is limited by the thickness of the epitaxial layer (of order of several micrometers). This results in the typical achievable signals generated by minimum ionising particles from few hundreds up to 1000 electrons. Therefore, reduction of noise sources is one of the critical issues in the design of CMOS sensors. Despite low MIP signal, the signal-to-noise ratio up to 40 has been demonstrated for CMOS MAPS [20, 54].

Although the CMOS sensors were being developed within the SUCIMA project [18], they were not easy to implement in the beam monitor application. The reason is that conventional CMOS MAPS are not suitable for the detection of the particles distinguished by a short range in silicon. If the backplane of such a sensor is exposed to short range particles (for example low energy electrons), they lose all their energy in the inactive volume of the sensor and do not generate measurable signal. Thus, in

[1]Research and development towards integration of fully CMOS readout circuitry in the cell of CMOS MAPS is also carried on [51], but these works are at early stage.

order to detect short range particles, the CMOS sensors have to be back-thinned up to the epitaxial layer. This process is expensive and it is not well established. It is also contrary to fully commercial approach of the CMOS MAPS.

3.2.2 DEPFET Detectors

Another highly developed solution of monolithic active pixel detectors is the DEPleted Field Effect Transistor (DEPFET). The operation principle of this device is presented in figure 3.4. The DEPFET pixel detector consists of a matrix of p-channel field effect transistors (JFET or MOSFET) manufactured on a n-type fully depleted substrate with the nominal thickness of 300 μm. When a particle passes through the sensor, it creates electron-hole pairs in the lightly doped substrate. The generated electrons drift towards the potential minimum that is formed by a sideward depletion and an additional phosphorous implantation (so called internal gate), and become accumulated. As the result of the charge accumulation at the internal gate, the drain current of the transistor is modulated. The sensor readout is performed by switching on the external gate of the selected transistor in the sensitive matrix.

During the readout of the DEPFET detector, the charge stored at the internal gate is not removed, which means that the readout is non-destructive and can be repeated several times. However, it results also in filling up of the internal gate by the signal charge and thermally generated electrons. For this reason, a positive voltage signal has to be periodically applied to the "clear electrode" in order to empty the internal gate.

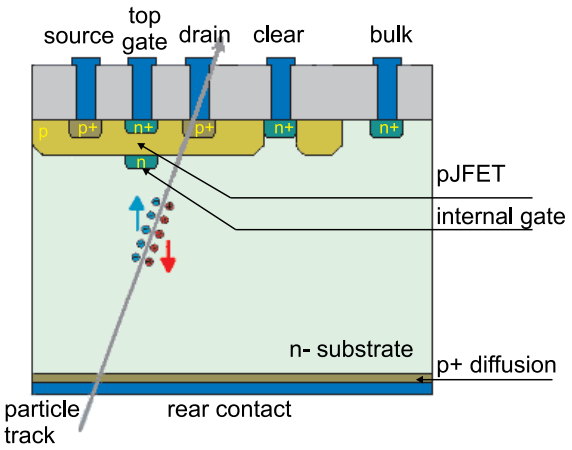


Figure 3.4: Cross-section of a DEPFET pixel sensor.

Although the DEPFET sensor allows integrating first amplifying transistor in the detector cell, it does not allow implementing more advanced signal processing within the cell and it requires separate steering and amplification integrated circuits for proper operation. The technology of the DEPFET is non-standard, which increases the cost of the detector development. Nevertheless, the DEPFET sensors offer excellent noise performance and readout pitch down to 24 μm [55]. They proved to be an efficient tool of autoradiography [56], astronomical X-ray imaging [57] and particle tracking [58].

Chapter 4

Monolithic Active Pixel Detector in SOI Technology

The existing solutions of active pixel silicon detectors were summarized in previous chapter. Although the presented approaches are well established and their efficiency in particles detection has been demonstrated, all of them have some specific disadvantages. The hybrid detectors do not allow obtaining thin devices, while monolithic detectors exclude more advance signal processing in the detector cell (DEPFET sensor) or produce lower MIP signals and are less suitable for the detection of particles with a short range in silicon (CMOS sensors). For this reason, the research works on new active pixel detectors are carried on. In this chapter, the solution of a monolithic active pixel detector that exploits silicon on insulator technology for the integration of a particle detector with readout electronics will be introduced. The technical details of the detector realization together with the potential advantages of the new device will be discussed.

4.1 Integration of Radiation Detector and Readout Electronics in SOI Substrate

A common silicon on insulator (SOI) wafer consists of a thin layer of single-crystal silicon separated from a bulk silicon substrate by an electrically insulating layer – typically silicon dioxide[1][6]. In standard integrated circuits, the top silicon film, called

[1]There are also technologies in which the single-crystal silicon film is formed over insulating substrate, such as quartz, sapphire, zirconia, etc., but these technologies are not proposed for manufacturing of monolithic active pixel sensors.

device layer, is used for manufacturing of electronic devices, while the bottom silicon substrate, called support layer or handle wafer, acts only as a mechanical support. The multilayer structure of the SOI wafer may be, however, exploited for the design of monolithic active pixel sensors in the way presented in figure 4.1. The main idea is the utilization of the silicon support layer as the radiation sensitive substrate of the monolithic detector and the fabrication of the readout electronics in a conventional way in the device layer.

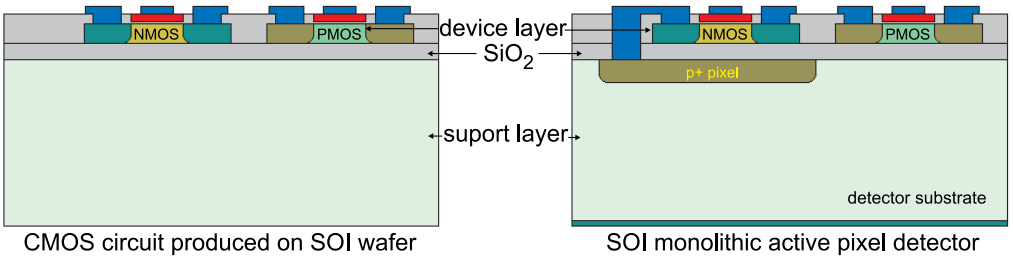


Figure 4.1: SOI technology for the realization of monolithic active pixel detecotrs: a conventional integrated circuit and a radiation detector produced on an SOI wafer.

4.2 SOI Wafers for Monolithic Pixel Detectors

The integration of a particle sensor and front-end electronics in the SOI substrate is not trivial. On the contrary to the conventional integrated circuits, the detector applications require substrates characterized by high quality of both device and support layer. Very important role plays also the quality and the reliability of the buried oxide layer (BOX), which should ensure perfect isolation between the electronics and the sensing part of the SOI detector. Last but not least, the chosen SOI substrate should permit using high resistivity handle wafers and low resistivity device layers to fully benefit from the SOI approach.

At present, most of the commercially available SOI wafers are produced using SIMOX or wafer-bonding techniques. The basics of both processes and their suitability for the production of monolithic active pixel detectors of the ionising radiation will be considered in the following paragraphs.

SIMOX Process

SIMOX – separation by implantation of oxygen – is a mature and well established method of the SOI wafer production. It bases on the implantation of oxygen ions below the surface of a silicon wafer. The implantation is usually performed at the temperature of 500°C to 600°C to avoid amorphizing the silicon overlayer. It is followed by high temperature annealing (typically at 1350°C [59, 60]), which leads to the formation of a buried oxide layer (BOX) and heals most of the silicon crystalline damages caused by the implantation. In modern SIMOX techniques, multiple implantation and annealing steps are usually performed and BOX growing is fulfilled by internal oxidation (ITOX) [59, 60, 61]. The ITOX process relies on thermal oxidation of the SOI wafer at temperature of about 1350°C, which is accompanied by the penetration of small fraction of oxygen into silicon and the formation of the internal thermal oxide at the silicon-oxide interface. This improves the buried oxide stoichiometry and increases its overall thickness.

The major challenges of the SIMOX process are formation of the BOX layers with adequate dielectric characteristics and preservation of the single crystalline nature of the silicon film. The development of low dose SIMOX processes, characterized by implantation doses of oxygen ions of order of few times 10^{17} cm^{-2}, allowed achieving high quality device layers with the dislocation densities as low as 10^{3} cm^{-2} [59, 62]. The low dose implantation results, however, in formation of thin buried oxide layers (typically 100 nm to 150 nm), which may be not sufficient for the realization of the proposed monolithic active pixel detectors due to possible cross-talk between the readout electronics and the detector active volume. Another problem associated with the SIMOX process is the risk of formation of silicon pipes in the buried oxide. The silicon pipes are continuous regions of silicon extending throughout the BOX. They may cause undesirable electrical short between the device and support layers of the SOI wafer. Although the reported densities of the silicon pipes are below 0.1 cm^{-2} [61] for modern SIMOX processes, these defects may still reduce the achievable manufacturing yield in the case of monolithic active pixel detectors since the structure areas of order of at least several square centimetres are required for most particle detector applications.

Wafer-Bonding

Wafer-bonding is an alternative method of the SOI wafers production. During this process, a thermally oxidized silicon wafer is bonded to another oxidized or bare silicon wafer. At the room temperature, the flat and smooth surfaces of the wafers are mainly connected by the Van der Waals forces or hydrogen bonds and water molecules.

The bond energy of the Van der Waals forces is low (of order of 7.5 mJ/m^2 [59]), and thus, it is expected that the hydrogen bonds and the water molecules play more important role in the bonding process. Forming of such bonds is possible due to the presence of OH groups on the surface of the wafers after standard RCA cleaning procedures[2] and water rinse. The coating hydroxyl groups attract each other and form hydrogen bridges. The reported bond energy is of order of few dozens of mJ/m^2 directly after contacting the wafer surfaces and reaches the maximum value of about 100 mJ/m^2 after annealing at room temperature [59].

In order to obtain better mechanical strength, the bonded pair is subsequently annealed at elevated temperatures. When the temperature increases from 20°C to 300°C, the water initially trapped between the bonded surfaces diffuses through the oxides to the silicon-oxide interfaces where the following reaction takes place:

$$Si/SiO_2 + H_2O \rightarrow SiO_x/SiO_2 + H_2$$

and additional thin oxide layer is produced. Further heating up to the 800°C removes remaining water from the bond interface and the following reaction that begins to fuse the bonded wafers is initiated:

$$Si-OH + HO-Si \rightarrow Si-O-Si + H_2O$$

The water produced in this reaction causes further oxidation of the silicon. As the temperature increases to 1100°C, the complete closure of the wafer interfaces occurs by coupling of the rest of the hydroxyl groups and the diffusion of hydrogen into the silicon bulk [59].

After the fusion process, one of the bonded wafers is thinned down to form the thin silicon film in which the electronic devices can be produced. This is usually performed in one of the following processes: grinding and chemical-mechanical polishing, back-etching (BESOI), plasma assisted chemical etching, bond and selective etching of

[2]RCA clean – industry standard for removing contaminants from a wafer. It includes 3 basic steps: organic clean, oxide strip and ionic clean.

porous silicon (e.g. ELTRAN® process) or implant enhanced wafer splitting (e.g. Smart Cut® technique). The details of these methods may be found in [6, 59, 60]. Depending on the applied thinning method, device layer non-uniformities from $\pm 0.5\mu$m (for grinding and polishing) down to ± 2 nm (for ELTRAN [60]) may be achieved.

Since in the wafer-bonded substrates, the device layer and the support layer originate from two separate silicon wafers, tailored resistivity of the latter can be used taking into account the specific aspects of the radiation detector implementation. In particular, the same materials as used for hybrid detectors production - high resistivity Float Zone (FZ) silicon, Czochralski (CZ) high resistivity silicon or oxygenated Float Zone silicon - can be used as the handle wafers. This make the wafer-bonding technique especially attractive for manufacturing of the introduced above monolithic active pixel detectors realized SOI technology. Further advantage of the bonding method is larger flexibility in the choice of the desired buried oxide and silicon film thicknesses. As it will be discussed later, the thickness of these layers is an important parameter, which must be optimized in order to keep the cross-coupling between the detector substrate and the readout electronics of a monolithic sensor at reasonably low level. Wafer-bonded SOI substrates distinguish also by good breakdown characteristics of the BOX layers. As the buried oxides originate from a thermal oxidation, they contain very few silicon inclusions and practically no pipe defects. The typical electrical breakdown fields of the buried oxides of the bonded wafers are approximately twice higher than those of SIMOX wafers [60, 62].

4.3 New Solution of SOI Monolithic Detector

The mentioned above characteristics of the wafer-bonded SOI substrates, together with the affordable cost and availability of the wafers on the market, have motivated the development of new monolithic active pixel detectors. The solution of the proposed device is presented in figure 4.2.

The sensor exploits commercially available SOI wafers. The radiation sensitive part is manufactured in a high resistivity ($4-10$ kOhm $\cdot$ cm), 400 μm thick support layer of the SOI wafer and it has a conventional form of a matrix of p^+-n junctions. Since the usage of ready-made bonded wafers excludes any wafer pre-processing before bonding, the detector p^+ pixels are implanted only in small cavities etched down in the silicon film and the BOX, and cannot be expanded further below the buried oxide. The pixel obtained in such a way is much smaller than the total detector cell, which dimensions

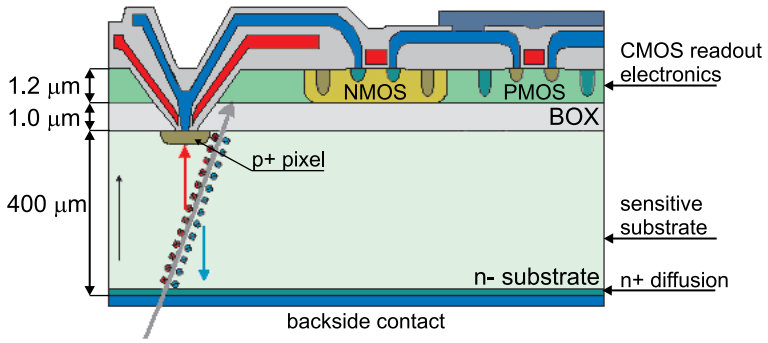


Figure 4.2: Cross-section of a monolithic active pixel detector realized in silicon on insulator technology.

are determined by the area required for the realization of a readout channel. The charge collection from the entire volume of the detector substrate is achieved through the extension of the electric field between neighbouring pixels. However, it can be expected that such a detector configuration will slightly lengthen collection time of the charge generated in between pixels and the readout electronics bias may interfere the distribution of the electric field close to the substrate-buried oxide interface.

In order to allow detection of the particles with a short range in silicon (for example alpha particles or low energy electrons used in the light ion beam monitor), the detector backplane is biased by a shallow n^+ ohmic contact and thin metalization. In the produced SOI detector prototypes, backside solid metalization layers with the thickness from 100 nm to 300 nm or metal meshes with rectangular holes were used.

The front-end electronics of the SOI detector is manufactured above the detector substrate in a low resistivity, 1.2 μm thick device layer. The device layer and the detector substrate are isolated by 1 μm thick BOX. The buried oxide and the silicon film are etched down at the points where the readout channels have to be connected with the associated sensing diodes by a metalization line.

The readout electronics and the detector diodes are DC coupled, which means that the detector p^+ pixels are biased directly by the input of the readout channels. DC coupling reduces the number of technological steps required for the sensor manufacturing, but complicates the design of the front-end electronics. The readout channel has to be able to sink the detector leakage current flowing into the input node along with the usable signal generated by traversing particles.

An important feature of the proposed sensor is the use of relatively thick silicon device layer and buried oxide. Such an approach allows reducing the cross-talk between the electronics and the detector substrate without necessity of the implementation of

any sophisticated shielding structure. One can see that the silicon film, the buried oxide and the detector substrate form a capacitor that couples the radiation sensitive and readout parts of the monolithic sensor. When a voltage pulse is applied to the silicon film, a charge signal is injected through the buried oxide into the detector substrate. As the injected charge is proportional to the value of the coupling capacitance, it is inversely proportional to the thickness of the dielectric layer. Thus, using thicker buried oxides reduces the cross-talk between the device and support layers.

The cross-talk is further reduced by avoiding changes of the voltage level at the electronics side of the coupling capacitor. This is achieved by using thick, densely biased electronics substrate. As presented in figure 4.2, the device layer in the proposed solution of the SOI sensor is so thick that the drain and source diffusions do not reach the buried oxide. It translates into significantly enhanced effectiveness of the transistor bulk polarization in comparison with the conventional SOI technologies.

The presented solution of the monolithic active pixel detector has several remarkable advantages. Since the proposed device uses a high resistivity detector substrate, it may operate at full depletion, just like a conventional hybrid detector. When high voltage (of order of 100 V) is applied to the detector backplane, practically the whole sensor volume constitutes the active region and the MIP signal as high as 29 300 electron-hole pairs is expected for the nominal sensor thickness of 400 μm. This value is approximately 20 times higher than achievable with the CMOS monolithic active pixel detectors.

If necessary, the SOI detector may be also thinned down. Since in the SOI sensors the charge signal is proportional to the sensor thickness, this parameter can be optimized for the particular application in term of the material budged and the desired signal-to-noise ratio. Existing technologies set the limit of thinning down to about 50 μm, but it is usually acceptable for inner detector systems of future high energy physics experiments.

Another attractive feature of the SOI sensor is the separation of the detector and electronics substrates, which allows using standard complementary MOS circuits in readout cells. It translates into increased flexibility of the front design in comparison with the DEPFET or CMOS monolithic sensors. In particular, the integration of signal processing (i.e. amplification, pedestal correction, filtering, discrimination, digitisation, etc.) directly in the readout cell is only restricted by the maximum available area for the single channel of a pixel detector and the limited access to deep submicron technologies

for the SOI sensor production. In the future, the possibilities of the implementation of advanced front-end electronics in the sensor cell may be extended by the developments of multilayer SOI wafers [63].

The readout electronics of the SOI detector is also expected to be inherently more resistant for Single Event radiation Effects (SEE). These transient effects are triggered by high energy particles traversing through the active substrate of electronics devices. The high density of the electron-hole pairs generated along the high energy particle track leads to the distortion of the electric field and the collection of a large amount of charge by the sensitive nodes of the electronic circuits. Typical results of the SEE are Single Event Latch-up (SEL - radiation induced switching on of a parasitic thyristor) and Single Even Upset (SUE - change of the logical state at an internal node of a digital circuit). Typical SOI technologies are characterized by high immunity to the SEE effects due to the reduction of the silicon volume in which the radiation generates charge carriers and the suppression of the parasitic thyristor structure [64]. In the case of the proposed SOI sensor, the elimination of the latch-up effect is not possible because of the use of a semi-bulk technology with junction isolation for the electronics production. Nevertheless, manufacturing of the CMOS devices on a silicon film still reduces the number of the charge carriers generated in the transistor body; consequently, the rate of the SEE should be reduced in comparison with the conventional technologies.

The major disadvantage of the SOI monolithic active pixel detectors is the fact that the production of these sensors requires a dedicated, non-standard process. Beside increased costs and complexity of the development, it usually does not allow following the dynamic progress that occurs in the field of commercial technologies. Non-standard technologies often suffer from larger device parameters variations, longer awaiting times for completing technological runs and limited access to the reliable technological files and circuit libraries for the computer aided design. However, many of these limitations may be overcome once the stage of large volume production is reached.

4.4 Verification of SOI Sensor Concept by Device Level Simulations

The concept of the new monolithic active pixel sensor that was introduced in previous section required extensive verification. In modern semiconductor industry, a common and efficient method of a device validation is the simulation performed with

the usage of a technology CAD (TCAD) software. Such a simulation allows better understanding of the device physics and examining its performance before entering the prototyping stage. It plays also an important role in the layout optimisation of the new device. For this reason, device level analyses of the SOI sensor were performed with the use of ISE-TCAD package - a set of tools for the simulation of technological processes and semiconductor structures provided by ISE (Integrated System Engineering)[3] [65]. A simplified sensor model was built and the most specific aspects of the monolithic active sensor realization were subsequently addressed in the simulations.

4.4.1 Device Geometry and Physical Model

The ISE-TCAD software allows design and analysis of two and three dimensional models. The latter are usually more suitable for pixel detector simulations due to more accurate modelling of the device geometry. It is especially relevant when the influence of the sensor layout on its performance has to be investigated. Nevertheless, the 3-D simulations are time consuming and are often impossible due to the hardware limitations. Therefore, a simplified, two dimensional model of the SOI sensor was used in majority of the simulations. The sensor model designed using the DEVISE editor from the ISE-TCAD package is illustrated in figure 4.3-a. It consists of three pixel diodes with the implantation widths of 20 μm and pitch of 150 μm. In order to simulate the presence of the readout electronics in the device layer, p-well and n-substrate contacts are formed above the BOX in the gaps between the detector diodes. The given geometry represents a worst-case situation, where the wells are formed far from the centres of the pixel implantations. The model boundary and the doping profiles are defined in agreement with technological data provided by the Institute of Electron Technology in Warsaw and are illustrated in figures 4.3-b and 4.3-c. The thicknesses of the device, BOX and support layers for the examined structure are given in figure 4.2.

For the described above geometry, a grid file, containing the mesh of discrete points for which the device properties were to be defined, was generated by the MASH tool. In order to ensure satisfactory simulation accuracy, the device mesh was refined (down to 50 nm) in the strategic regions of the device: close to the buried oxide–silicon interface, around pixel implantations and in the areas of high doping gradient or electric field. Such a sensor structure was subsequently analysed with the

[3]Integrated System Engineering (ISE) is currently a part of Synopsys, Inc.

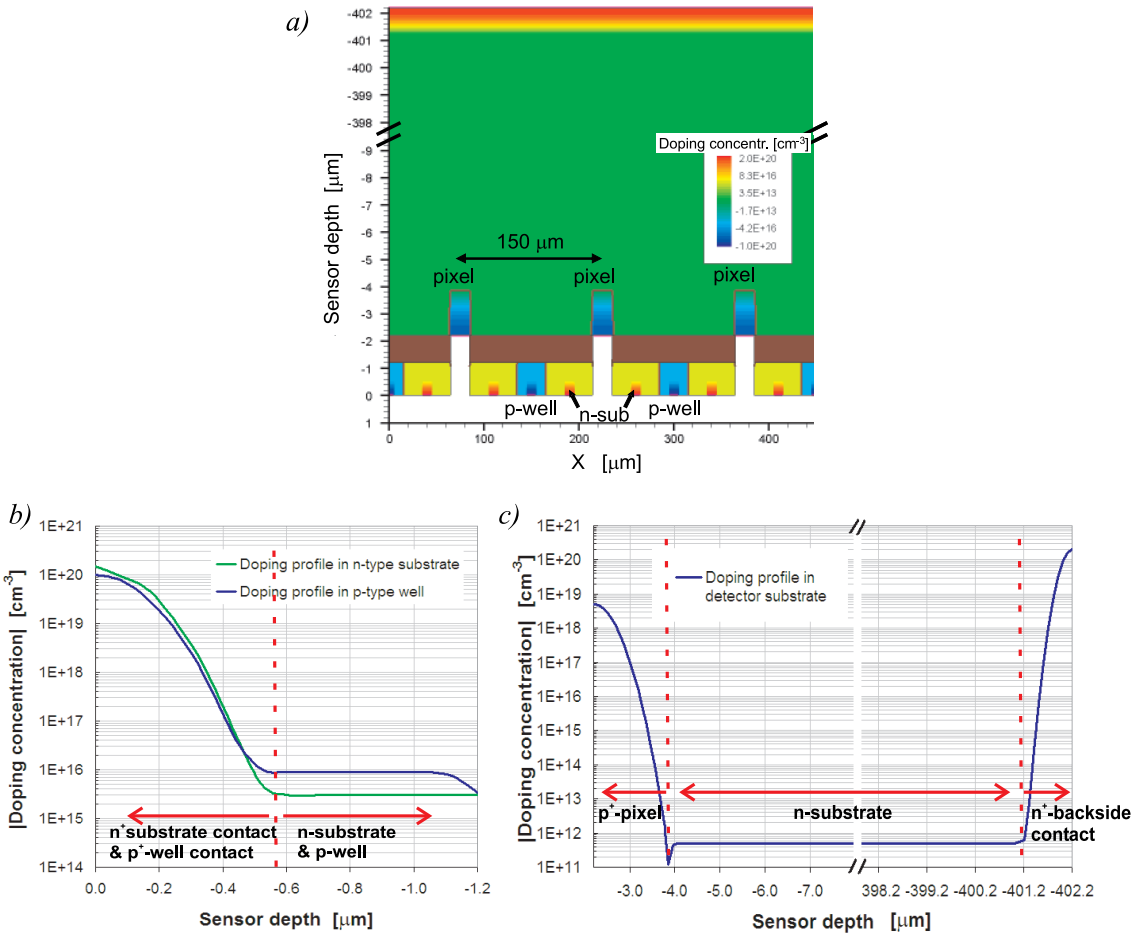


Figure 4.3: 2D model of the SOI sensor used in simulations: a) device geometry and b) doping profiles in the device layer and c) in the detector sensitive substrate.

use of DESSIS - multidimensional device and circuit simulator from ISE. The physical behaviour of the designed device was simulated using standard, isothermal drift-diffusion transport mode along with the following physical models:

- Slotboom band gap model
- Masetti doping-dependent mobility model
- Canali high field mobility saturation model
- Lombardi mobility degradation model at interfaces
- Shockley-Read-Hall (SRH) doping-dependent recombination model

Short descriptions of the above models and their default parameters are given in appendix A. Since in the case of the SOI sensors, the quality of the interface between radiation sensitive substrate and BOX plays an important role, the physical properties of the oxide-silicon interface were also modelled by incorporating the surface SRH recombination model and the surface fixed charge with uniform concentration. Basing on the results reported in literature [62, 66], the recombination velocity and fixed charge concentration were set to 3000 cm/s and $10^{11}/\mathrm{cm}^2$, respectively. The results of the simulations obtained using the described sensor geometry and the physical model are discussed in the following.

4.4.2 Simulation of Interaction between Readout and Sensitive Part of SOI Sensor

As presented in previous section, the basic charge collection mechanism in the introduced SOI sensors is the same like in hybrid detectors. Nevertheless, in the case of the monolithic sensors, in which the detector sensitive part and the readout electronics are manufactured in direct proximity, additional effects that may interfere with the sensor operation have to be investigated. In particular, the cross-coupling between both parts of the monolithic device and the effect of relatively large distance between pixel implantations on the charge collection have to be studied to validate the concept of the new device.

First effect that should be addressed is the influence of the electronics bias on the potential distribution in the detector sensitive substrate. As presented in figure 4.2, in the proposed solution of the SOI detector, the source and drain implantations are terminated far from the buried oxide interface and their biasing should not affect significantly the potential distribution in the detector. Nevertheless, the voltage signals applied to the electronics substrate and wells may still change the operating conditions of the radiation sensitive part of the sensor. Especially dangerous are these areas where the p-type wells are created above the gaps between the pixels. These wells have to be connected to the lowest potential in the circuit, and thus, they may cause local potential minima, which disturb the collection of the charge generated underneath. For this reason, the sensor geometry illustrated in figure 4.3 was simulated for the device electrodes biased with constant voltages: 0 V for the pixels and the wells, 5 V for the device substrate contact and 100 V for the detector backplane.

The potential distribution obtained by solving the Poisson equation for the investigated structure is presented in figure 4.4. In this figure, potential minima around the pixel implantations are clearly visible. Nevertheless, more careful analysis of the potential distribution close to the interface of the buried oxide indicates the effect of the electronics bias on the detector operation. Potential pockets below well implantations may be observed in figure 4.5-a, where the potential distribution in the sensor sensitive substrate at the depth of 5 μm below the buried oxide is illustrated.

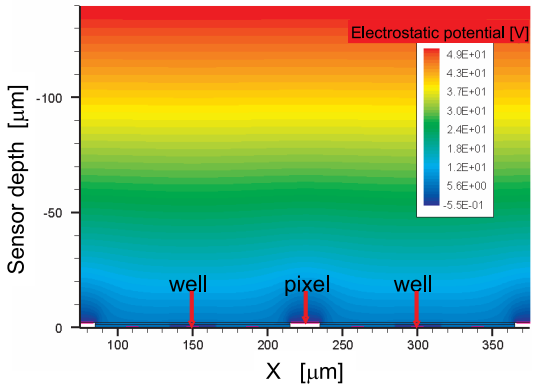


Figure 4.4: Potential distribution in the central part of an SOI detector without buried implanted layer (up to the sensor depth of 140 µm). Results are obtained for pixel and p-well bias of 0 V, device substrate bias of 5V and backplane bias of 100 V.

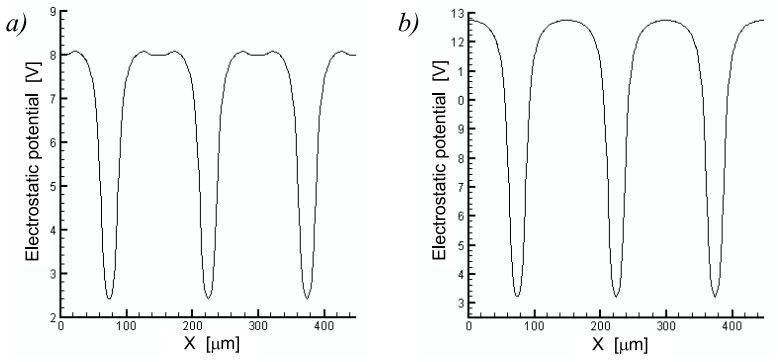


Figure 4.5: Potential distribution at the depth of 5 µm bellow BOX: a) for the structure without buried arsenic implanted layer, b) for the structure with buried arsenic implanted layer. Centers of the pixel implantations at 75 µm, 225 µm and 375 µm; p-well implantations biased with 0 V - over the middle of the gaps between pixels.

The problem of the local potential minima in the sensor sensitive substrate below the buried oxide layer may be solved in various ways. The simplest solution may be increasing the device layer thickness and in this manner moving the bottom of the p-well away from the BOX interface. In the case of the technology available at IET, it would require device film thickness of at least 3 μm. Such a thick device layer translates into larger silicon area necessary for formation of the V-shape pixel cavity.

Another solution of the problem may be modifying the basic SOI sensor structure presented in figure 4.2 by applying special shielding structure between the readout and radiation sensitive regions. As illustrated in figure 4.6-a, such a shielding structure may be realized in multilayer SOI technology. In such a case, an intermediate, highly doped, silicon layer is connected to constant potential and screens the detector substrate from the readout electronics. This solution requires non-standard SOI wafers, and thus, has not been explored. An alternative method, which may allow realization of the shielding structure without changing the sensor layout or the technology, is exploitation of commercially available wafers with buried implanted layers [67]. As illustrated in figure 4.6-b, the buried implanted layer, called also blanket, is a shallow, highly doped region formed at the interface between the device layer and the buried oxide. In standard applications of the SOI technology, it is used for gettering impurities in the silicon film [68]. In the case of the SOI detector, it may act also as a shield between the electronics and the detector substrate. The result of the exploitation of the blanket

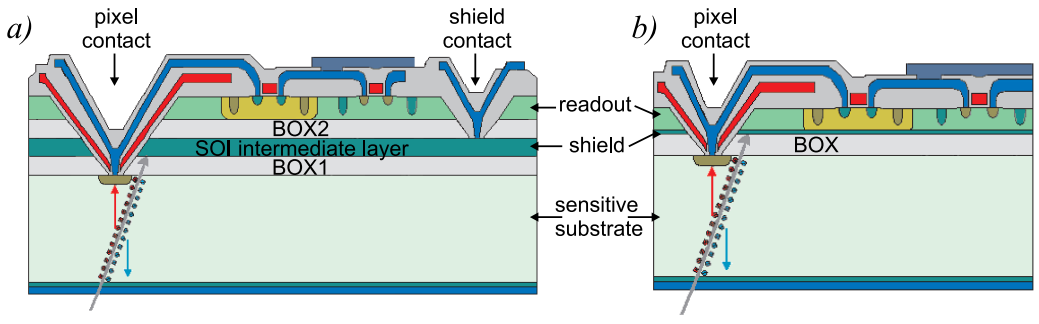


Figure 4.6: Proposals of SOI sensors with special shielding structures for minimizing the interaction between the readout electronics and the detector radiation sensitive substrate; a) shielding structure realized in SOI multilayer technology, b) shielding structure based on the wafers with buried implanted (blanket) layers.

layer is illustrated in figure 4.5-b, where the potential distribution for the structure with an additional buried arsenic implantation, characterized by the top concentration of $10^{18}/\mathrm{cm}^3$, is depicted. As presented, the harmful distortion of the potential distribution bellow the well implantations is not visible for the device with the blanket implanted layer.

Apart of the discussed above problems, the possibility of the crosstalk between the readout electronics and the detector sensitive volume has to be investigated for monolithic sensors. As reported in [8] and [69], sudden changes of the voltage signals in the front-end electronics may cause injections of parasitic current signals into the detector active substrate through the buried oxide layer. There are several possible sources of such interferences in the SOI sensors: the digital control part of the readout sensor, the steering lines of the readout cells and these electrodes of the transistors in readout cells on which the potential may suddenly change during the circuit operation (e.g. channel selection switches). The crosstalk between the readout circuit and the detector substrate, similarly as the crosstalk between the analogue cells and the digital part of the readout electronics, may be reduced to a large extend by a proper layout design of the monolithic active pixel sensor – routing digital signals by couples of parallel lines with opposite polarization and placing digital control blocks outside the detector guardring. These techniques will be described in details in next chapters. The crosstalk may be additionally minimized by dense biasing of the device layer along the digital lines. In such a way the impedance between the electronic substrate below the signal line and the circuit ground is reduced. The low impedance between these nodes makes the significant portion of the parasitic current flow to the circuit ground rather than to the detector sensitive substrate through the impedance formed by the buried oxide capacitance. The effectiveness of this method was confirmed by the simulation of the device model similar to the one presented in figure 4.3. The simulated structure was supplemented by a single 4.5 μm wide and 150 μm long metal line placed over 1 μm thick field oxide, at the distance of 10 μm from the bulk contact and 40 μm from the edge of the pixel implantation. This configuration is representative for the layout of the SOI sensors. In order to simulate circuit operation, a pulse-like signal with the amplitude of 5 V and the rising/falling edges of 500 ps was applied to the metal line and a mixed-mode analysis was performed with DESSIS. The current signal and the integrated charge obtained on the pixel electrode are presented in figure 4.7. It may be observed that a transient current signal is induced on the pixel electrode, but the integral of that signal after approximately

5 ns from the edge of the voltage pulse has a negligible value. Similar result was obtained in another simulation, in which a pulse voltage signal with the amplitude of 1 V was applied to a drain implantation with dimensions of 9 μm x 9 μm. Thus, according to the simulation, the dense electronic substrate polarization, along with the use of thick device layers and buried oxides, may be considered an efficient method of reducing interaction between the front-end electronics and the sensitive substrate of the sensor operating in the charge integration mode.

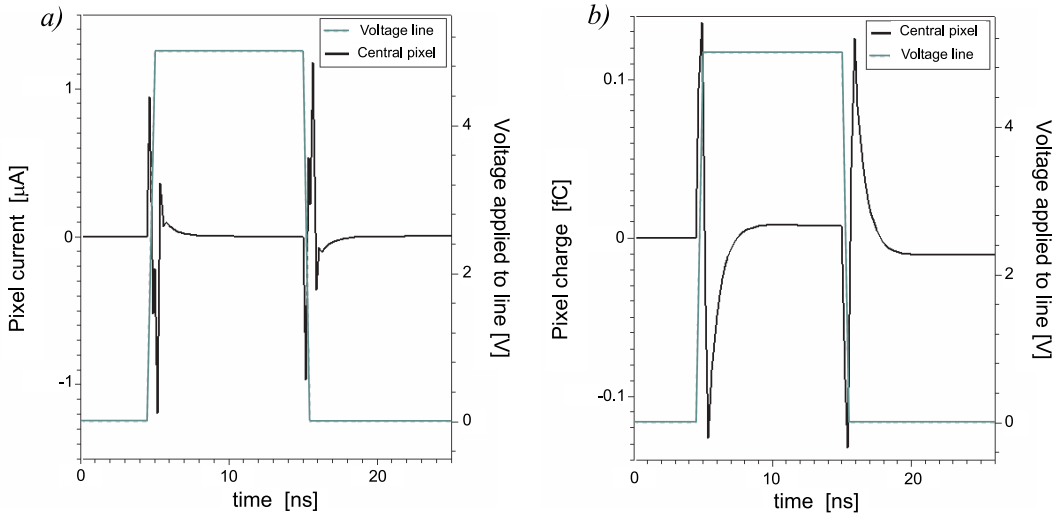


Figure 4.7: a) Simulated current signal induced on a pixel electrode and b) corresponding integrated charge resulting from the voltage pulse signal applied to a metalization line.

4.4.3 Simulation of Charge Collection

Another group of the SOI sensor simulations concerned the charge collection properties of the new particle detectors. The primary goal of such simulations was investigating how the total amount of the collected charge and the charge collection time depend on the ionising particle trajectory and the detector bias. Performed simulations were also guidelines for the proper design of the SOI sensor prototypes and showed the directions of further improvements of the detector structure.

In order to simulate the charge collection prosperities of the monolithic active pixel sensors manufactured in SOI technology, the geometry presented in figure 4.3 was used. Since only standard SOI wafers were expected to be available for the sensor prototyping, the analysed device model did not include any shielding structure. For

the simulation of a minimum ionising particle (MIP), the method described in [54] was exploited. The proposed approach bases on the alpha particle model implemented in the ISE-TCAD. The charge generation rate in this model is given by:

$$G(x,y,t) = \begin{cases} \frac{a}{s\sqrt{2\pi}}\, e^{-\frac{1}{2}\left(\frac{t-t_m}{s}\right)^2} e^{-\frac{1}{2}\left(\frac{x}{w_t}\right)^2} \left[c_1 e^{\alpha y} + c_2 e^{-\frac{1}{2}\left(\frac{y-\alpha_1}{\alpha_2}\right)^2} \right] & \text{for} \quad y < \alpha_1 + \alpha_3 \\ 0 & \text{for} \quad y \geq \alpha_1 + \alpha_3 \end{cases} \tag{4.1}$$

where x and y are the coordinates perpendicular and parallel to the particle track and remaining coefficients are parameters of the alpha particle model. The parameter t_m is the time of the generation peak, while w_t defines the radial distribution of the generated charge along the particle track. The maximum of the Bragg peak α_1 is fitted by a polynomial function of the particle energy E:

$$\alpha_1 = a_0 + a_1 E + a_2 E^2 \tag{4.2}$$

and the parameter c_1 is expressed by:

$$c_1 = e^{\alpha(\alpha_1[10\text{MeV}] - \alpha_1[E])} \tag{4.3}$$

At last, the scaling factor a is determined from the following condition:

$$\int_0^\infty \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} G(x,y,t) = \frac{E}{E_{e-h}} \tag{4.4}$$

where E_{e-h} is the energy required for the generation of a electron-hole pair in silicon. After modifying the default model parameters to the values given in table 4.1 and applying the particle energy of 2.88 MeV, the chare generation rate of 76 electron-hole pairs per micrometer of the particle track and the radial charge distribution of 0.75 μm are achieved.

Table 4.1: Coefficients of the alpha particle model used for simulation of MIP particle.

Parameter	w_t	c_2	α	a_0	a_1	a_2	E_{e-h}	s
Unit	[cm]	[-]	[cm^{-1}]	[cm]	[cm/eV]	[cm/eV^2]	[eV]	[s]
Value	75×10^{-6}	0	1×10^{-15}	1	0	0	3.6	1×10^{-10}

The analysis of the charge collection in the SOI sensors was performed by transient simulations in DESSIS. The detector bias and the impact position were parameterized and a single interaction of the minimum ionising particle with the sensor material

was considered for every set of the simulation parameters. The corresponding value of the collected charge was calculated by the integration of the electrode current. The initial solution for the given bias conditions was calculated using the quasistationary analysis, and then the transient analysis was performed assuming the charge generation time of 1 ns. The distribution of the electrostatic potential and the electric field were recomputed at each step of the transient simulation along with the electron and hole continuity equations.

An exemplary result of the transient simulation, obtained for the detector bias of 100 V, is presented in figure 4.8. The figure illustrates the densities of electrons and holes in the sensor material after the passage of an ionising particle through the centre of the pixel implantation. As presented, after the charge carriers generation, the electrons and the holes begin drifting towards the n^+ backside contact and the p^+ pixel implantation, respectively. As the result of higher mobility, the electrons are collected faster than the holes. Along with the drift transport, partial diffusion of the charge carriers also occurs, but due to relatively large distance between pixels, the total charge is collected on a single pixel diode.

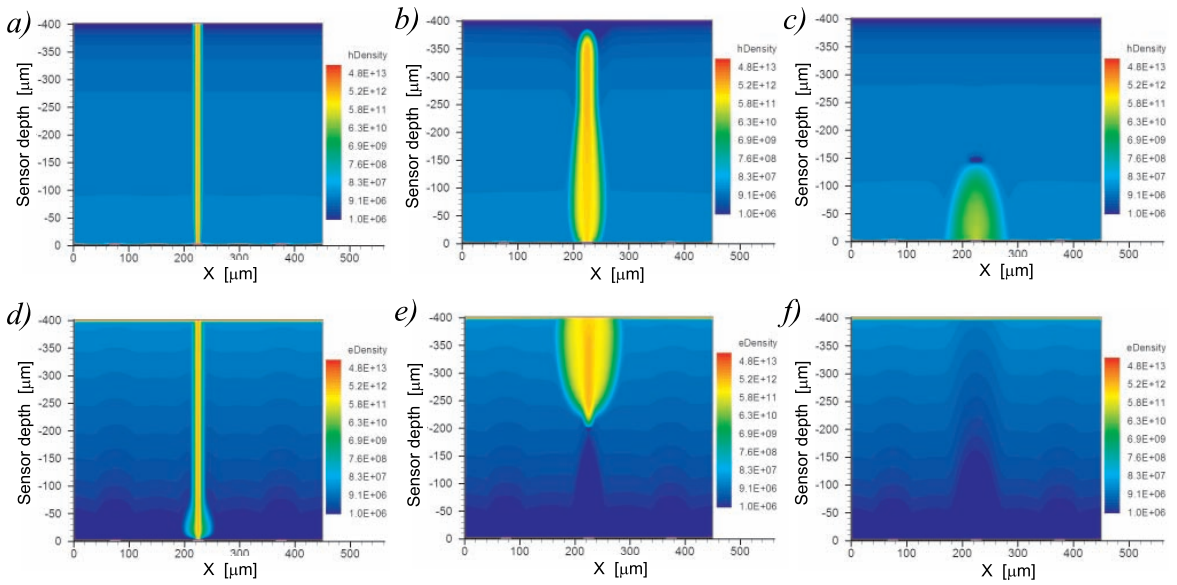


Figure 4.8: Hole density in the SOI sensor substrate: a) immediately after the charge generation by a MIP, b) after 9 ns and c) after 49 ns; electron density in the SOI sensor substrate: d) immediately after the charge generation by a MIP, e) after 9 ns and f) after 49 ns.

More general results of the charge collection simulations are depicted in figures 4.9 - 4.11. As presented, the number of the pixels in cluster, the current signal shapes, the total amount of the collected charge and the charge collection time depend both on the detector bias and the impact position.

Figures 4.9-a and 4.9-b show the shape of the pixel current and the corresponding integrated charge for different values of the voltage V_{DET} applied to the sensor backplane. The results are illustrated for the MIP traversing the detector substrate perpendicularly to the sensor surface and directly below the central pixel of the structure given in figure 4.3. As expected, when the radiation sensitive substrate of the sensor is underdepleted, the charge collection is incomplete. The amount of the collected charge is approximately proportional to the thickness of the depleted region, which is described by equation 2.17. For assumed simulation parameters, the total sensor volume becomes depleted at the detector polarization slightly higher than 60 V. Thus, almost all the generated charge (98.2%) is collected for this detector bias after the simulation time of 400 ns. As given by equations 2.35 and 2.36, the charge collection time is significantly extended due to the low electric field in the sensor substrate ($E_{min} \approx 0$). Further increase of the reverse bias voltage V_{DET} increases the electric field beyond the value required for the full depletion of the detector. For

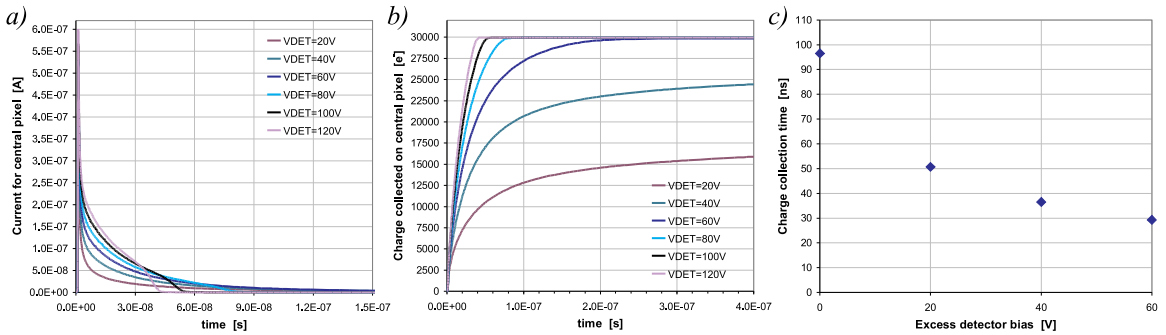


Figure 4.9: a) Simulated current signal induced on the electrode of the central pixel for different values of voltage V_{DET} applied to the sensor backplane, b) corresponding integrated charge and c) charge collection time versus detector bias beyond full depletion voltage. Results obtained for MIP particle traversing the sensor substrate at the position X=225 μm.

such bias conditions and the charge generated directly below the pixel implantation, the shape of the current signal at the sensor cathode may be approximated by the superposition of the current signals given by formulas 2.33 and 2.34. As presented in figure 4.9-c, the charge collection time[4] diminishes significantly as the excess detector bias increases.

The simulation results presented in figure 4.9 correspond to the special case when the charge is generated directly below the pixel implantation. Since the SOI sensors are characterized by large spacing between the pixel implantations, more general analysis of the charge collection process is necessary. Figure 4.10 shows the shape of the current signals induced on the detector cathodes for different impact positions and the detector bias of 100 V. As presented, when a MIP particle traverses the substrate of the SOI sensor far from the pixel implantations, the current pulse formed on the detector electrode is delayed and broadened. In such a case, the charge generated in the sensor active volume first rapidly drifts in electric field towards buried oxide interface, but then it is slowly transported along the surface of the BOX towards the electrodes. The charge collection is additionally disturbed by the local potential minima below

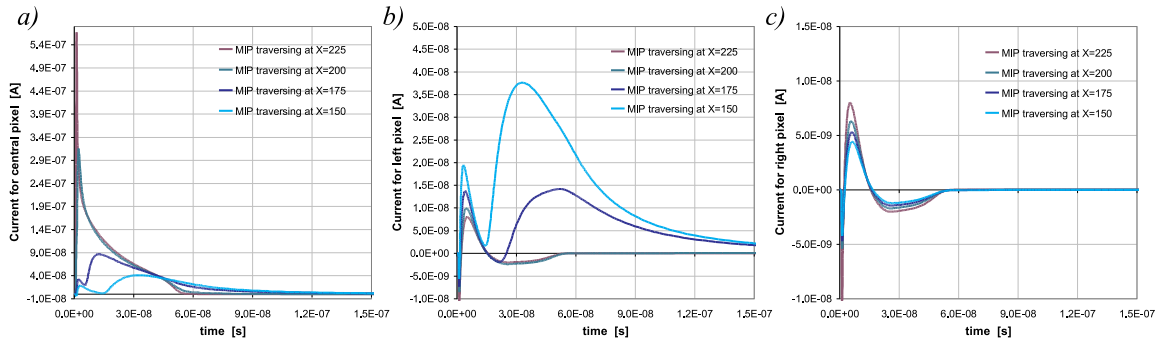


Figure 4.10: Current signals induced on the sensor electrodes for MIP particles traversing the sensitive substrate at different positions: a) signal induced on central pixel, b) left pixel and c) right pixel. Results obtained for V_{DET}=100 V.

the p-wells. Thus, as illustrated in figure 4.11, the charge collection time becomes significantly longer and the charge-sharing between neighbouring cells occurs. Since the recombination velocity is much higher close to the buried oxide interface, part of the generated charge is also lost before it reaches the sensor electrodes. Nevertheless, even

[4]Charge collection time is computed as the time required to gather 90% of the generated charge.

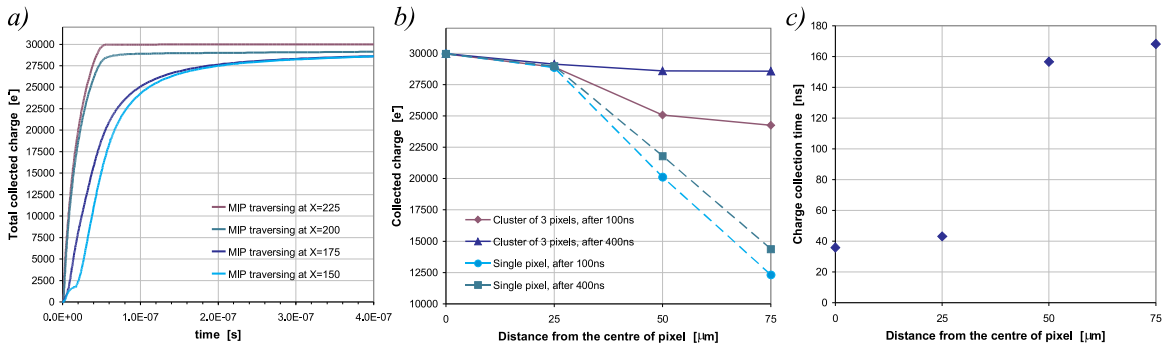


Figure 4.11: a) Time dependence of the total charge collected in the cluster of three neighbouring pixels for MIP particles traversing the sensitive substrate at different positions; b) collected charge for a cluster of three pixels or a single pixel and c) charge collection time as a function of particle impact position with reference to the centre of the pixel implantation. Results obtained for V_{DET}=100 V.

if the charge is created in the middle of the gap between two neighbouring pixels, 95 per cent of it become collected after the time of 400 ns for given simulation parameters.

It should be pointed out that the long charge collection time and the charge loss are mostly related to the large distance between the pixels implantations in the SOI sensors manufactured in the available technology. Once a deep submicron process becomes available for the SOI sensor production, improvement of the charge collection time and the efficiency may be expected. Further improvement of the charge collection properties of the SOI sensor may be possible by applying a shielding structure between the device and support layers of the SOI substrate. As discussed earlier, using such a structure assures overcoming the problem of the distortion of the potential distribution below the p-well implantations. In addition, biasing the device substrate and the shield with higher voltage than the pixel electrodes allows shifting carriers transport deeper into sensor sensitive substrate. The effect of the usage of the shielding structure in the form of blanket implantation on the charge collection properties is illustrated in figure 4.12. One observes that after the simulation time of 400 ns the total amount of the collected charge increases to 99.7 percent and the charge collection is reduced from 168 ns to 122 ns for V_{DET} = 100 V and the worst case situation when the charge is generated in the middle of the gap between two pixel implantations.

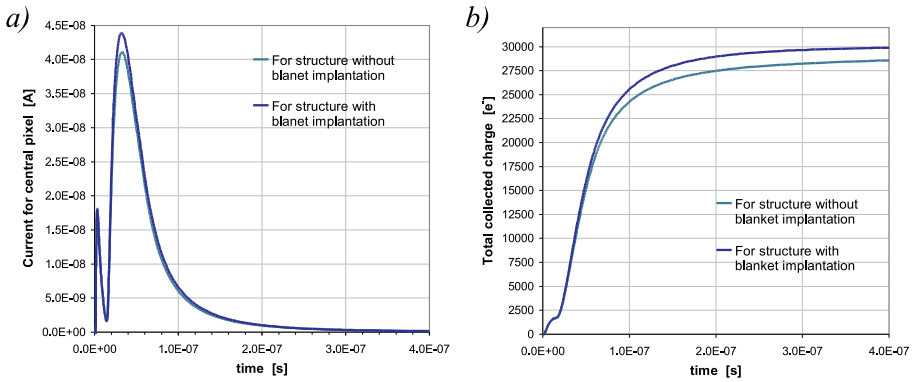


Figure 4.12: a) Current signal induced on the electrode of the central pixel for structures with and without burried implanted layer and b) total collected charge for cluster of three pixels. Results obtained for a MIP particle traversing the sensor substrate at the position X=225 μm and for V_{DET}=100 V.

4.5 Comparison with Previous Research Works on SOI Detectors

The idea of the integration of a radiation detector and front-end electronics in an SOI substrate arose more than ten years ago at IMEC (Interuniversity MicroElectronics Center) [70]. The SOI technology was then projected to be an attractive option of manufacturing monolithic active pixel sensors. It was expected that SOI sensors might provide almost 100 % fill factor[5] and increased radiation hardness. A practical solution of the SOI detector was proposed by the collaboration of RD19 group from European Laboratory of Nuclear Physics CERN and IMEC [7, 8]. The research group studied the suitability of SIMOX, ZMR (zone melt recrystallization) and bonded SOI wafers for the realization of monolithic fully depleted active pixel sensors. Due to the most promising results, the wafer-bonded substrates were chosen for final device processing.

As illustrated in figure 4.13, the major difference between the solution proposed by the RD19 collaboration and the device introduced in this thesis is the method of decoupling of the readout electronics and the detector substrate. Instead of using thick device and buried oxide layers, the RD19 group proposed an electric shield between the electronics and the sensitive volume [8]. The shield together with the pixel

[5]Fill factor is defined as a ratio of the sensitive and total cell areas.

implantations were formed in the support layer below the readout electronics, and thus, wafer pre-processing before bonding was required. Due to processing problems, the developments of the RD19 group were abandoned at an early stage and the proposed ideas have not found practical implementation.

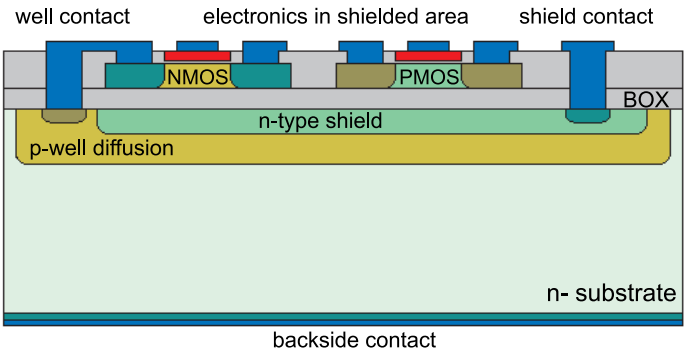


Figure 4.13: The idea of the SOI detector with embedded electrostatic shield [8]

Later works in the field of the SOI monolithic active pixel sensors were focused on the development of visible light sensors. The photodetector solutions reported in [71, 72] based on manufacturing of sensing diodes in a low resistivity supporting layer of an SOI wafer (SIMOX or wafer-bonded). In contrast to the SOI detector solution introduced in this thesis, they did not allow operation at full depletion. Recently, there was also an effort to realize a visible light sensor using a fully depleted pinned photodiode created in the support layer of a wafer-bonded structure [73]. In the case of this device, only the small volume of the pinned diode constituted the sensitive substrate. Additionally, this device did not provide 100 % fill factor.

Chapter 5

Development of SOI Detector Technology

Manufacturing of the monolithic active pixel detectors based on SOI technology requires a non-standard technology, which integrates a pixel manufacturing technique with a typical CMOS process. The major challenge of such technology is processing from both sides of the buried oxide and preserving high quality of detector diodes despite manufacturing steps of CMOS devices in the upper silicon layer. Technology used for prototyping of the proposed SOI sensor was developed at the Institute of Electron Technology in Warsaw [50, 74, 75]. It was verified and characterized in terms of the transistor and passive components characteristics and the quality of the detector junctions [76, 77, 78]. In the following sections, the key features of the SOI detector technology together with the characterization of the devices produced in this process will be discussed.

5.1 Choice of SOI Substrates

The technology of the SOI detector was developed using SOI wafers provided by SOITEC and Analog Devices Belfast[1]. These two types of wafers differed mainly by the thinning down method applied by the vendor.

The SOITEC wafers are produced using the Smart Cut® process, invented at CEA-LETI [59]. The key feature of the process is the formation of the thin silicon film by splitting the donor wafer along an ion implanted plane. In the commercial version

[1]Analog Devices Belfast has been closed. Currently wafers produced in the same process may be purchased from IceMOS Technology (www.icemostech.com)

of the process, the hydrogen ions are implanted into a thermally oxidized wafer at the typical dose above 5×10^{16} cm^{-2}. After conventional wafer-bonding, the bonded pair is annealed at the temperature of $400-600$°C, which leads to wafer splitting along the hydrogen layer. Subsequent touch-polishing allows achieving surface roughness comparable with bulk wafers. The Smart Cut process offers very well defined absolute thickness and uniformity[2] of the device layer (down to ± 5 nm [79]), but the availability of the substrates with high resistivity FZ support layers is strongly limited. For this reason, the SOITEC wafers were only used for setting up the CMOS SOI technology and the complete SOI sensors were produced on the wafers provided by Analog Device (AD).

The AD wafers are thinned down by grinding and chemical-mechanical polishing. This method is characterized by worse absolute film thickness control and surface roughness than implant enhanced wafer splitting. The device layer tolerance of ± 0.5 μm (according to vendor specification [80]) for the nominal thickness of 1.5 μm translates into spread of the transistors characteristics and variations of the shape of the cavity in which the connection between the detector diode and the readout electronics is formed. As it will be presented in next chapter, it also result in variations of the charge-to-voltage conversion gain of the basic configuration of the SOI sensor. Nevertheless, the flexibility of the combination of the handle/device layers resistivity and thickness is a great advantage of the Analog Devices wafers. The specification of the wafers used for the SOI sensor production is summarized in table 5.1. As the minimum device layer thickness of the AD wafers is 2 μm, this layer had to be further thinned down by 0.5 μm at IET using oxidation and etching.

5.2 Technology of SOI Detector

The technology developed for the purpose of the SOI sensor manufacturing is similar to the standard CMOS process commonly used at IET. This process offers minimum feature size of 3 μm, one polysilicon and two metalization levels. The new technology is characterized by the realization of semi-bulk MOS devices on a thick SOI substrate. The isolation between transistors is provided by the junction isolation and the body/well contacts are preserved like in standard bulk technologies. As mentioned, using thick film SOI substrates and body/well contacts reduces the coupling between

[2]Thickness uniformity is defined as 3 times standard deviation for all wafers.

Table 5.1: Specification of the wafers used for the SOI detector manufacturing [80, 75].

Handle Layer	Thickness	400 μm
	Dopant type	N-type
	Resistivity	$>$ 4kOhm $\cdot$ cm
	Growth method	FZ
	Crystal orientation	$<$100$>$
BOX	Thickness	1.0 μm
Device Layer	Thickness	2.0 μm
	Thickness tolerance	$\pm$0.5 μm
	Dopant type	P-type
	Resistivity	9-13 kOhm $\cdot$ cm
	Growth method	CZ
	Crystal orientation	$<$100$>$

the detector substrate and the readout electronics. It also simplifies the design of the analogue circuits as the kink and history effects [6], which are known in typical partially depleted SOI (PD-SOI) technologies, should be efficiently suppressed. On the other hand, the devices produced in such a process do not benefit from the reduction of the source-to-substrate and drain-to-substrate capacitances and more compact layout, which is the major disadvantage of the proposed technology.

In comparison with the standard CMOS technologies, the manufacturing of the SOI detector requires additional steps for the pixel implantation and the formation of the openings in the silicon film and the buried oxide. It also imposes very strict limitations on the sequence and the duration of high temperature processes. Therefore, the technology developed at the IET is very complex and consists of more than 120 individual processes. The cross-sections of the device at specific manufacturing steps are presented in figure 5.1.

As presented, the technological sequence is organized in such a way that long lasting high temperature processes, like dopants rediffusion after well implantation and field oxidation, are performed before BOX opening above the future pixel junction area. One of the last operations within the sequence is the formation of backside contacts. Such a procedure allows obtaining shallow contacts, which are necessary for the detection of low energy beta radiation. The total thermal budget of the whole technological

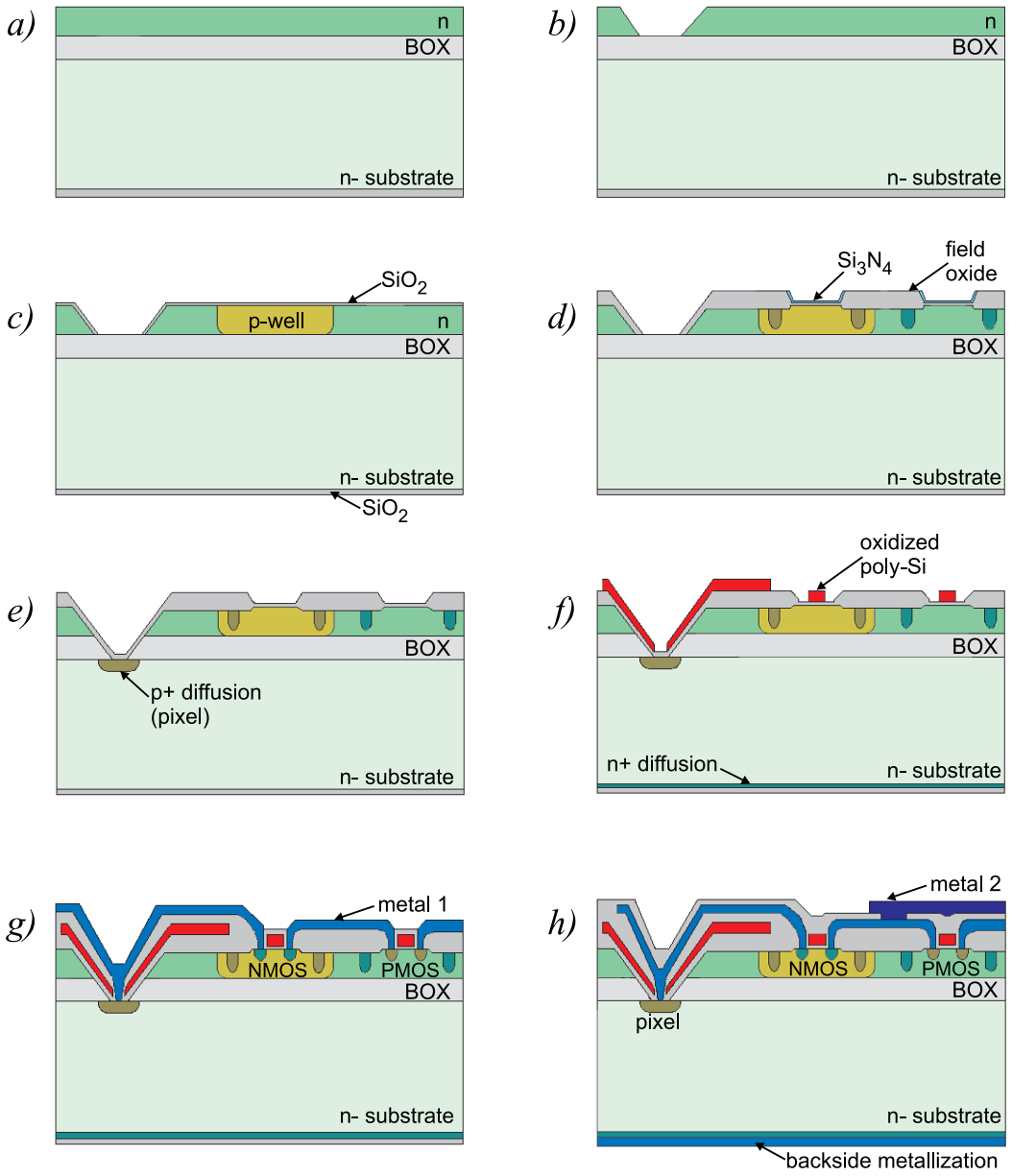


Figure 5.1: The fabrication steps of the SOI detector. The SOI detecotr cross-section after a) doping of the device layer for PMOS transistors, b) etching pixel cavities in silicon device layer above the BOX, c) creation of the p-well in the device layer, d) active area definition, channel stoppers formation and field oxidation, e) pixel junction fabrication and gate oxidation, f) poly-Si deposition, photolithography and oxidation, g) photolithography of metal 1 and h) final device.

sequence is optimized to avoid distraction of the high resistive detector material and to provide optimal junction depth in the CMOS active layer. In view of the limited thickness of the device layer in SOI substrates, the total amount of the silicon consumed during oxidation is also taken into account.

One of the important issues of the SOI detector processing is the reliability of the connection between pixel diodes and readout channels. Since the proposed solution of SOI sensor exploits relatively thick device and buried oxide layers, the metal path between both parts of the active sensor has to pass through the steps of significant height. In order to ensure continuous electrical paths, the pixel cavity has a V-shape created by anisotropic etching of the silicon with $<100>$ orientation. In addition, the surface of the cavity walls is smoothed out by a polysilicon coat, which also prevents the detecting diode from possible contamination during the subsequent technological processes. The resulting structure of the pixel–readout input connection together with its microscopic photograph is presented in figure 5.2.

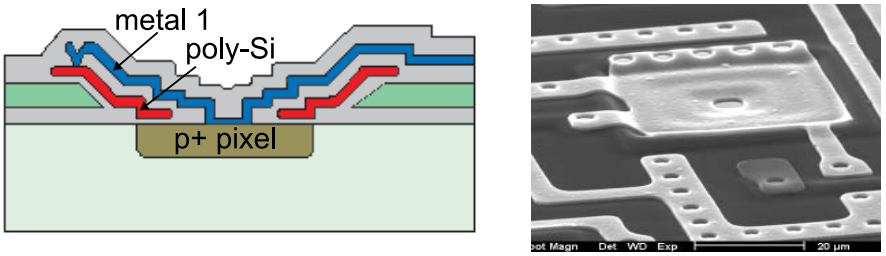


Figure 5.2: The cross-section of the connection between the pixel and the readout channel together with its microscopic photograph.

5.3 Technology Verification and Characterization

Every new semiconductor technology requires verification and characterization. These processes are extremely important in view of an inadequate number of experimental data and reliable device models for the technologies being still under development. In the case of non-standard technologies – like the technology of the SOI monolithic active pixel sensor – the validation process becomes even more important due to the presence of non-CMOS devices (such as detector junctions), the possible coupling between the detector and electronics active layers and the consequences of the usage of a semi-bulk CMOS technology with junction isolation on the SOI substrate

with limited silicon film thickness. For this reason, dedicated test structures (called SUCIMA1 and SUCIMA2) were designed taking into account the specific aspects of the SOI sensor implementation [77, 78, 81, 82]. The design of the test structures was focused on these features of the new technology that are especially important for mixed-mode integrated circuits. Particular units of the test structure allowed the examination of the characteristics of basic elements of electronic circuits and pixel diodes, the evaluation of the device parameters mismatches, the investigation of the performance of electronic functional blocks and the comparison of the measured characteristics with the simulations results.

Since before the works on the test structures were started, neither the transistor models nor the design rules had existed for the new technology, the SUCIMA1 chip was designed using the transistor model parameters (level 3) and the design rules developed at IET for the standard bulk 3 μm CMOS process. In order to allow the automatic design rule check (DRC) and the device extraction from the layout, a set of technological files and scripts for the CADENCE environment was prepared. Apart of the standard masks used in the CMOS technology, the developed design kit contained also additional masks required for the detector diodes manufacturing.

The SUCIMA1 test structure was produced in several iterations that differed in the technological parameters (like implantation doses of the electronics bulk) and the SOI wafers sources (SOITEC, Analog Devices). Detailed wafer-level measurements were performed for several processed wafers with the identification numbers of PT29/2, PT28/2 and PT249. First two of them were produced on the SOITEC substrates with low resistivity support layers and were used for the SOI-CMOS technology arrangement. The last wafer was produced on the AD substrate with high resistivity support layer and was additionally used for the detector junctions measurements.

The SUCIMA2 test structure was designed after the basic technology verification had been completed and was produced together with large-scale prototypes of the SOI monolithic active pixel detectors. New model files, prepared according to the Spice level 3 transistor parameters extracted at IET for the SOI-CMOS technology, were used for the simulation of the elements of the test structure. The test structure was manufactured only at the peripheries of wafers, and thus, it could not be used for statistical measurements. The major role of the test structure was to allow crosschecking between different technological lots. With reference to SUCIMA1 test structure, it was supplemented with additional units for better detector junctions

characterization. It also contained elements for the future development of the SOI detector and its technology. Wafer level measurements of the SUCIMA2 test chip were performed for the wafers with identification numbers of 229 and 246.

Photographs of the manufactured SUCIMA1 and SUCIMA2 test structures are presented in figure 5.3, while the content summaries of these chips are attached in appendix B. The design and the measurement results of the particular elements of the test structures will be described in details in the following sections.

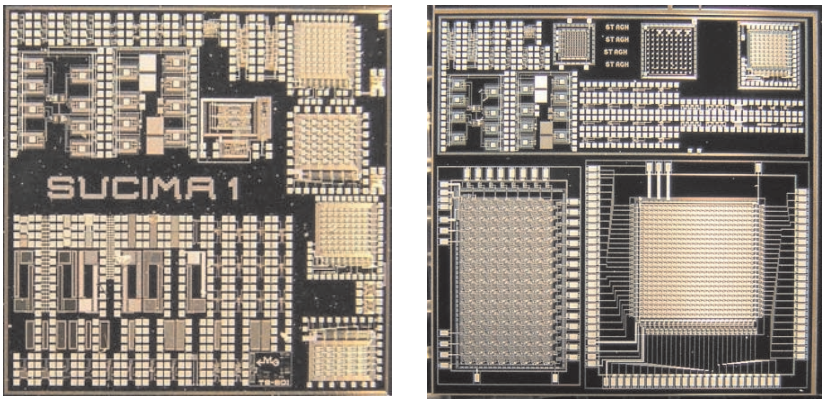


Figure 5.3: Photographs of the test structures used for the development of IET-SOI technology: SUCIMA1 (left) and SUCIMA2 (right) test chips.

5.3.1 Characterization of Standard CMOS Components

Stand-alone Transistor Unit

First unit of the test structure consists of ten differently sized NMOS and ten PMOS stand-alone transistors. The transistors have conventional rectangular shapes and they are grouped in several sets with common gate, body and source contacts and separate drain outputs. Most transistors are surrounded by guardrings to ensure good body or well polarization. Some of them have the dimensions typical for the readout applications. There are short but wide transistors (e.g. W/L = 20μm/3μm, 40μm/3μm) – used in the input stages, narrow transistors (e.g. W/L = 6μm/14μm) - used as resistors and long transistors (e.g. W/L = 20μm/10μm, 40μm/20μm) - common in current sources. In this part of the test structure, the basic characteristics MOS devices and the effectiveness of the transistor body biasing in the SOI technology were investigated. Transistor measurements were also guidelines for the development of the technology versions with adequate parameters for the SOI detector applications.

The characterization of the transistors produced on the SOI wafers was performed with the usage of a manual probe station and the HP4155A semiconductor parameter analyser controlled by a set of dedicated programs running under LabVIEW [83]. Families of the measured characteristics of NMOS and PMOS transistors are presented in figure 5.4. Since in the new SOI sensor technology, the contact to the transistor body is preserved, the characteristics have the shapes typical for bulk devices. Nevertheless, in view of the limited thickness of the device layer and the increased substrate sheet resistance, it might be expected that the effectiveness of the bulk polarization is reduced on the SOI wafers. For this reason, some additional measurements were performed in order to investigate the influence of the device layout and the bulk polarization on its characteristics.

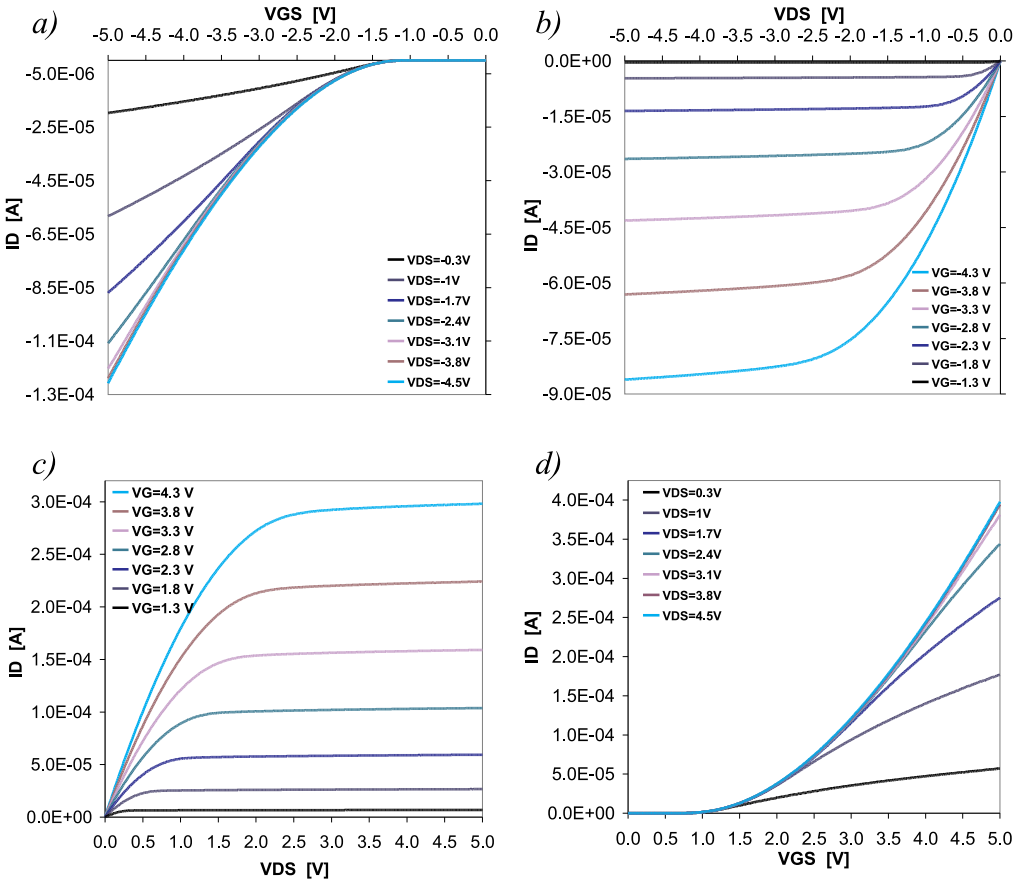


Figure 5.4: Characteristics of transistors produced on SOI wafers: a) transfer characteristics of NMOS, b) output characteristics of NMOS, c) transfer characteristics of PMOS and d) output characteristics of PMOS. Results obtained for device dimensions of $W/L = 20\mu\text{m}/10\mu\text{m}$.

Body contact geometry and body polarization effects

The effectiveness of the transistor body biasing was studied for three transistor layouts illustrated in figure 5.5: with the body contact along the transistor drain, across the gate and with the body contact in the form of a guardring. Performed measurements indicated dependence of the transistor characteristics on the body/well contact arrangement only for the first lot of the test structures (wafer PT29). For later iterations, all the devices layouts allowed effective bulk biasing. As an example, the comparison of the output characteristics obtained for the transistors produced on an Analog Devices substrate (wafer PT249) is presented in figure 5.6.

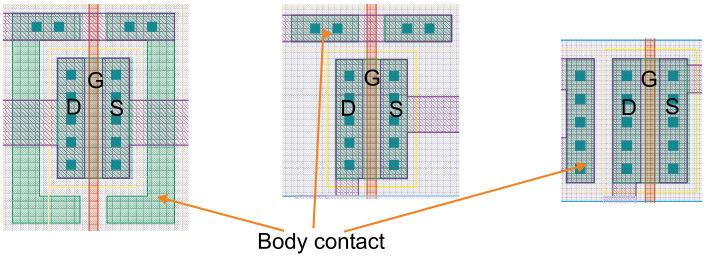


Figure 5.5: Layouts of transistors with dimensions of W/L = 40μm/3μm *and with different body contact arrangements - a) body contact in the form of a guardring, b) across the gate and c) body contact along the transistor.*

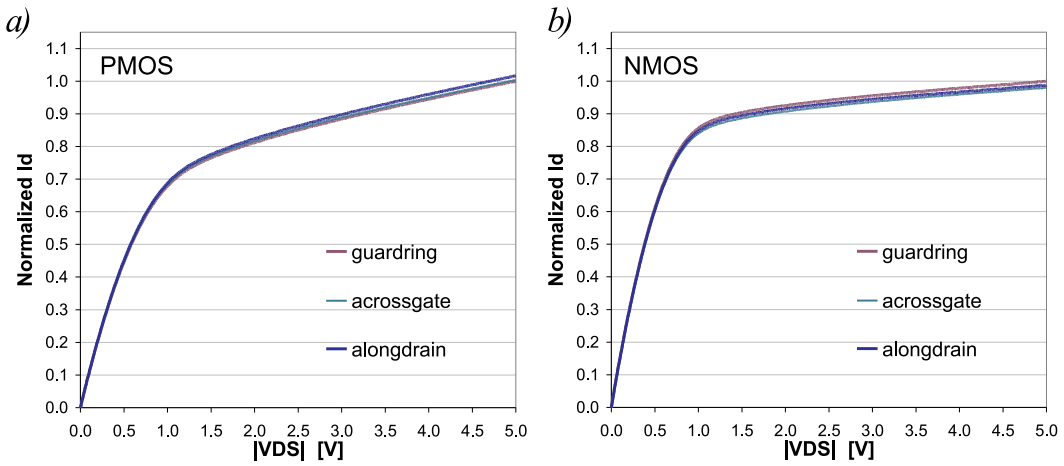


Figure 5.6: Normalized output characteristics of a) PMOS and b) NMOS transistors produced on an Analog Devices SOI substrate (PT249). Results presented for zero body-source polarization.

The studies of the body polarization effect required the measurements of the threshold voltages and their shifts for different body-source voltages. There are several methods of the threshold voltage V_T measurements [84]. One of them relies on the extraction of the threshold voltage from the transistor transfer characteristic $I_D(V_{GS})$ in the saturation region.

According to the simplest first-order model, the drain current I_D for the saturation region is given by the following formula:

$$I_D = \frac{\beta'}{2}(V_{GS} - V_T)^2 \tag{5.1}$$

where V_{GS} is the value of the gate-source voltage and β' is the current factor expressed by:

$$\beta' = \mu C_{ox} \frac{W}{L} \tag{5.2}$$

Quantities μ and C_{ox} in the above equation denote the channel carriers mobility and the gate oxide capacitance per unit area (5.31×10^{-8} F $\cdot$ cm^{-2} for the IET-SOI technology with oxide thickness of 65 nm). The value of the threshold voltage V_T depends on the body-source bias V_{BS} due to the changes of the thickness of the channel-bulk depletion layer, as it describes the formula:

$$|V_T| = |\mathrm{VT0}| + \mathrm{GAMMA}\left(\sqrt{|\mathrm{PHI}| + |V_{BS}|} - \sqrt{|\mathrm{PHI}|}\right) \tag{5.3}$$

where VT0, GAMMA and PHI are Spice model parameters representing: the threshold voltage V_{T0} at $V_{BS} = 0$, the body factor and the surface potential, respectively.

Using equation 5.1, the threshold voltage can be obtained from the intersection of the linear segment of the square root of the transistor transfer characteristic. This method is illustrated in figure 5.7. The measurements of the threshold voltage for various body-source voltages allow subsequently studding the effect of the transistor body polarization.

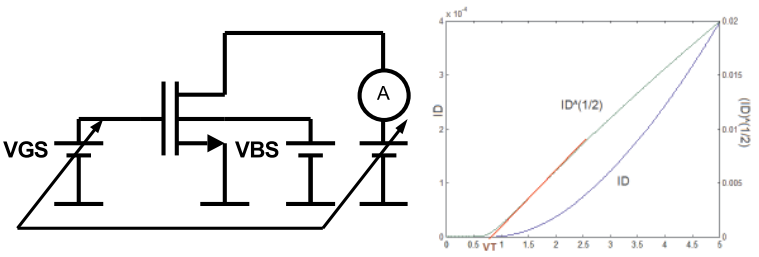


Figure 5.7: Threshold voltage measurements - connection diagram and extraction method.

The measurements of the threshold voltage versus source-body polarization were performed for several test structures on each tested wafer and the results were averaged. In order to investigate the influence of the transistor dimensions on the threshold voltage value and the body effect, differently sized transistors (W/L = 6μm/3μm, 20μm/10μm, 40μm/20μm) were included in these tests. From the results obtained for the largest transistors, the GAMMA and PHI parameters were extracted taking into account the relation between those quantities and the substrate doping concentration NSUB:

$$\text{GAMMA} = \frac{\sqrt{2\varepsilon_{Si}\varepsilon_0 \text{NSUB}}}{C_{ox}} \tag{5.4}$$

$$\text{PHI} = 2\frac{kT}{q}\ln\frac{\text{NSUB}}{n_i} \tag{5.5}$$

Extracted values of the GAMMA, PHI and NSUB parameters for different technological iterations along with other parameters determined for the transistors manufactured in the investigated process are summarized at the end of this section in table 5.4. The characteristics of the threshold voltage shift versus the bulk polarization, measured for transistors produced on both SOITEC (PT28) and Analog Devices (PT249) SOI substrates, are presented in figure 5.8. As illustrated, in the case of the PMOS transistors, the measured curves follow the theoretical fit (equations 5.3, 5.4 and 5.5) only for the large area transistors (W/L = 20μm/10μm, 40μm/20μm) and for a limited range of the body-source voltage. It may be expected that for higher values of the V_{BS} voltage, the body-source depletion zone of the PMOS transistor approaches the surface of the BOX and further changes of the body potential only slightly affect the threshold voltage. For NMOS transistor, the saturation of the V_T versus V_{BS} characteristic is not noticeable due to the higher p-well doping, and thus, slower expansion of the source-bulk depletion zone in the well material. Comparison of the characteristics depicted in figures 5.8-a and 5.8-c, as well as GAMMA factors extracted for PMOS transistors produced on the wafers PT28 and PT249 (0.64 and 0.43, respectively) confirms that the range of V_{BS}, in which the threshold voltage is efficiently modulated by the body polarization, is wider for the transistors produced on higher doped device substrates. It is worth to point out that the shape of the $V_T(V_{BS})$ characteristic of the PMOS transistor is not adequately modeled by a simple Spice model relying on the equation 5.3. It becomes important for those electronic circuits in which the body/well-source voltage changes during their operation (e.g. transmission gates and source followers).

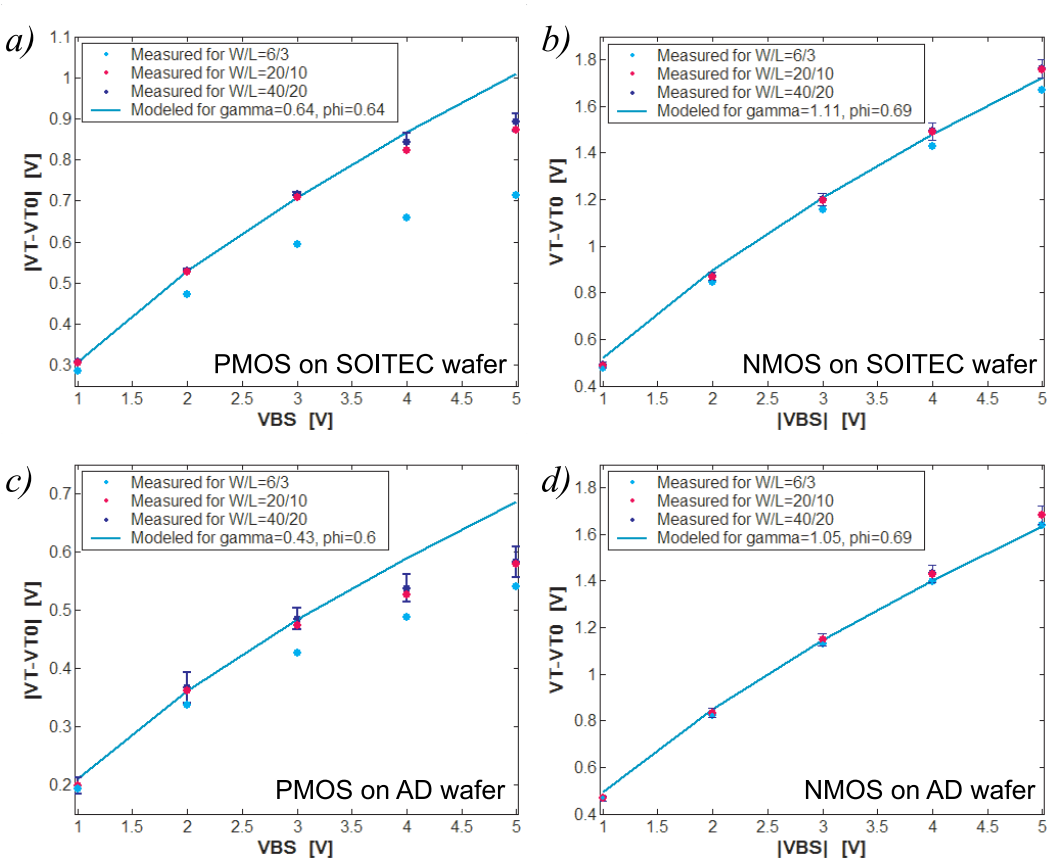


Figure 5.8: Threshold voltage shift (VT-VT0) versus body-source polarization (VBS) for transistors with different dimensions and located on the SOITEC wafer PT28/2 (a-PMOS, b-NMOS) and the AD wafer PT249 (c-PMOS, d-NMOS). For the transistors with dimensions of $W/L = 40\mu\text{m}/20\mu\text{m}$, error bars are added.

Choice of transistor operating point

Another branch of the measurements performed with the use of the stand-alone transistor unit of the SUCIMA1 test structure aimed at better characterization of PMOS and NMOS transistors at the saturation region. The main purpose of these measurements was the proper choice of the operating points of the transistors building readout circuits. In view of the lack of reliable device models for the new CMOS-SOI technology, the experimental extraction of such a small signal parameters as the transconductance and the output conductance, was necessary for the optimization of the readout design.

The characterization of transistors at the saturation region (i.e. for drain-source voltages V_{DS} higher than $V_{GS} - V_T$) required the examination of transistor parameters at both strong and weak inversion. As mentioned, the first-order expression of the transistor drain current at the saturation and the strong inversion is given by 5.1 and 5.2. The actual drain current is smaller than the first-order value and the $\beta'/(\frac{W}{L})$ parameter has to be replaced by a process current factor K'. The process current factor is always lower than the β' current factor divided by W/L ($K' < \mu C_{ox}$). As illustrated in figure 5.7, it can be extracted from the slope of the square root of the linear segment of the transistor transfer characteristic at the strong inversion. An alternative way to reduce the drain current value is to divide the β' factor in equation 5.1 by a correction factor $n > 1$. This leads to the following formula describing the transistor drain current at the saturation and the strong inversion:

$$I_D = \frac{\beta'}{2n}(V_{GS} - V_T)^2 = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2 \tag{5.6}$$

The correction factor n in the above equation is a function of the bulk-source voltage V_{BS} and is given by:

$$n = 1 + \frac{\text{GAMMA}}{2\sqrt{\phi_j - V_{BS}}} \tag{5.7}$$

where ϕ_j indicates the bulk-channel junction built in voltage.

Further correction of the first-order expression of the drain current involves the effect of the limited transistor output resistance r_{ds} (non-zero output conductance g_{ds}) at the saturation region. The limited output resistance at the saturation results from the extension of the drain-channel depletion layer and the reduction of the channel length with increasing values of the drain-source voltage V_{DS}. This effect is represented by the following expression:

$$I_D^{s.i.} = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \text{LAMBDA}\ V_{DS}) \tag{5.8}$$

in which LAMBDA is the Spice fit parameter that determines the slope of the transistor output characteristic $I_D(V_{DS})$.

Equation 5.8 is valid only for the gate-source voltage V_{GS} higher than V_{ON} approximated by:

$$V_{ON} \approx V_T + n\frac{kT}{q} \tag{5.9}$$

when the condition of the strong inversion is met. For the gate-source voltage close to the threshold voltage, the transistor enters the weak inversion region and the drain

current shows exponential behaviour, as given by the following formula:

$$I_D^{w.i.} = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS}}{nkT/q}\right)(1 + \text{LAMBDA}\ V_{DS}) \tag{5.10}$$

where I_{D0} is a process-dependent parameter. The n factor present in the above equation is the same as the correction factor in equation 5.6 and may be extracted from the slope of the logarithm of the transistor transfer characteristic at weak inversion.

Using equations 5.8 and 5.10, small signal transistor parameters at given operating point can be calculated. From the slope of the transfer characteristic, the transistor transconductance can be obtained in the following forms:

$$g_m^{s.i.} = K' \frac{W}{L}(V_{GS} - V_T) = 2\sqrt{\frac{K'}{2}\frac{W}{L} I_D^{s.i.}} \quad \text{for strong inversion} \tag{5.11}$$

$$g_m^{w.i.} = \frac{W}{L}\frac{I_{D0}}{nkT/q} \exp\left(\frac{V_{GS}}{nkT/q}\right) = \frac{I_D^{w.i.}}{nkT/q} \quad \text{for weak inversion} \tag{5.12}$$

$I_D^{s.i.}$ and $I_D^{w.i.}$ in the above formulas indicate the transistor drain current at the operating point for the strong and weak inversions, respectively.

Equations 5.11 and 5.12 allow deriving the transconductance-to-current ratios (called also transconductance efficiencies) that illustrate how efficiently the current is used to generate the transconductance. The transconductance-to-current ratios for the strong and weak inversions, respectively, are given by:

$$\frac{g_m^{s.i.}}{I_D^{s.i.}} = 2\sqrt{\frac{K'}{2}\frac{W}{L}\frac{1}{I_D^{s.i.}}} \tag{5.13}$$

$$\frac{g_m^{w.i.}}{I_D^{w.i.}} = \frac{1}{nkT/q} \tag{5.14}$$

Another important small-signal parameter of a transistor operating at the saturation region is the output resistance that can be obtained from the equations 5.8 and 5.10 in a common form:

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\text{LAMBDA}\ I_D^{sat}} \tag{5.15}$$

where I_D^{sat} indicates the transistor drain current at the operating point in the saturation region. Since the LAMBDA parameter in the above equation depends on the channel length L, it is more convenient to use a dimension independent parameter V_E to express the transistor output resistance in the following way:

$$r_{ds} = \frac{1}{g_{ds}} = \frac{V_E L}{I_D^{sat}} \tag{5.16}$$

The V_E parameter is called the Early voltage (in analogy to the Early voltage in bipolar transistor) and, taking into account the relation:

$$V_E = \frac{1}{\text{LAMBDA } L} \tag{5.17}$$

can be extracted by the measurements of the LAMBDA parameter for different transistor dimensions.

Since the derived above small-signal transistor parameters determine the gain and the noise performance of amplifying circuits, their dependence on the operating point has to be investigated. According to equations 5.11-5.14, the transistor transconductance at the weak inversion is directly proportional to the drain current, while at the strong inversion, it is proportional only to the square root of that current. The transistor output resistance is also larger at the weak inversion due to a low value of the drain current at this region. Thus, the weak inversion region is preferred for the high gain and low power operation. The input-referred spectral density of the channel thermal noise for the transistors working at the weak inversion is lower, too. Therefore, this region is especially attractive for the design of low noise electronics. Nevertheless, the high-frequency performance at the weak inversion is poor and the transistor parameters at this operating point are very sensitive for device mismatches. For this reason, it was decided that the readout electronics for the SOI detector should operate at the drain currents approximately an order higher than the currents corresponding to the transition from the weak to strong inversion.

In order to find such a transistor operating point, the characteristics of the transistors produced in the new CMOS-SOI technology were measured and analyzed. The region of the transition from the weak to strong inversion was traced and the dependence of the small signal parameters on the device operating point was investigated.

The transfer characteristics and the transconductances were measured for the transistors with dimensions of $W/L = 40\mu\text{m}/3\mu\text{m}$, which were expected to be used as input devices of readout electronics. The transfer characteristics in a logarithmic current scale and the square roots of the transfer characteristics obtained for the PMOS and NMOS transistors at $V_{DS} = 3.8$ V are presented in figure 5.9. The regions of the weak and strong inversions are marked on these plots. As presented, the transition from the weak to strong inversion occurs at the gate-source voltages of approximately -0.84 V for PMOS and 0.77 V for NMOS transistors, which corresponds to the drain currents of about 0.6 μA and 1.7 μA, respectively. Taking into account the possible mismatches

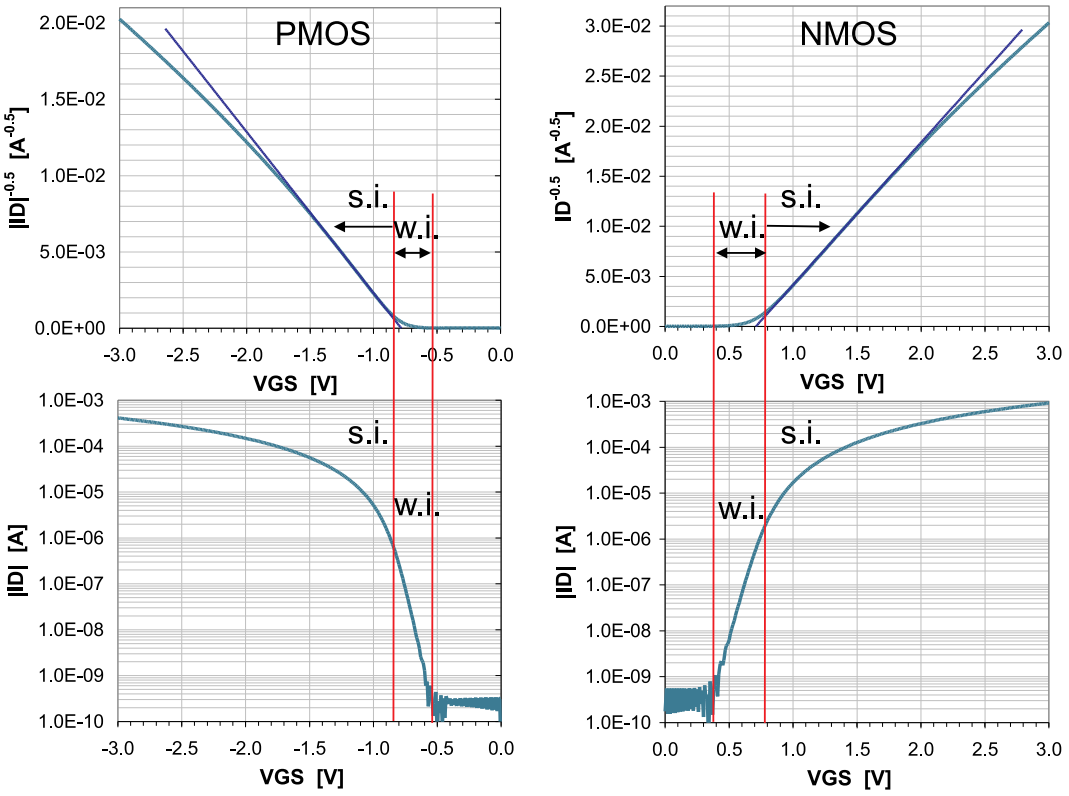


Figure 5.9: Transistors transfer characteristics $I_D(V_{GS})$ with square root and logarithmic current scale. Results obtained for PMOS and NMOS transistors with dimensions of $W/L = 40\mu\text{m}/3\mu\text{m}$, operating at the saturation ($|V_{DS}| = 3.8$ V) and produced on the wafer PT249. w.i. and s.i. indicate the weak and strong inversion.

of the parameters of transistors from different lots and the demands on the readout electronics performance, obtained results give the following ranges of the transistor operating points that should guarantee safe and proper operation the readout circuit:

$$1.0\text{ V} < V_{GS} < 1.2\text{ V}, \quad 6\ \mu\text{A} < I_D < 20\ \mu\text{A} \quad \text{for PMOS}$$

$$0.9\text{ V} < V_{GS} < 1.1\text{ V}, \quad 16\ \mu\text{A} < I_D < 30\ \mu\text{A} \quad \text{for NMOS}$$

The measured transfer characteristics allowed extracting some process dependent parameters that are present in equations 5.8 and 5.10. The process current factor K' and the threshold voltage V_{T0} were determined from the square root of the transfer characteristic, while the correction factor n was obtained from the logarithm of the transfer characteristic. Summary of the results is given in table 5.2.

Table 5.2: Extracted values of the K', n and V_{T0} parameters for NMOS and PMOS transistors with dimensions of $W/L = 40\mu\text{m}/3\mu\text{m}$ at $V_{BS} = 0$ V. Results obtained for typical transistors produced on the wafer PT249.

	K' [μA/V^2]	n	V_{T0} [V]
PMOS	16.8	1.44	-0.78
NMOS	30.4	1.77	0.71

As the transistor transfer characteristics allow only rough estimation of the safe transistor operating point, the exact choice of the drain current of the input device has to be made relying on the measurements of the transconductance and the output conductance. The transconductance and its efficiency versus the drain currents are presented in a bilogarithmic scale in figure 5.10. Changes of the slopes of the

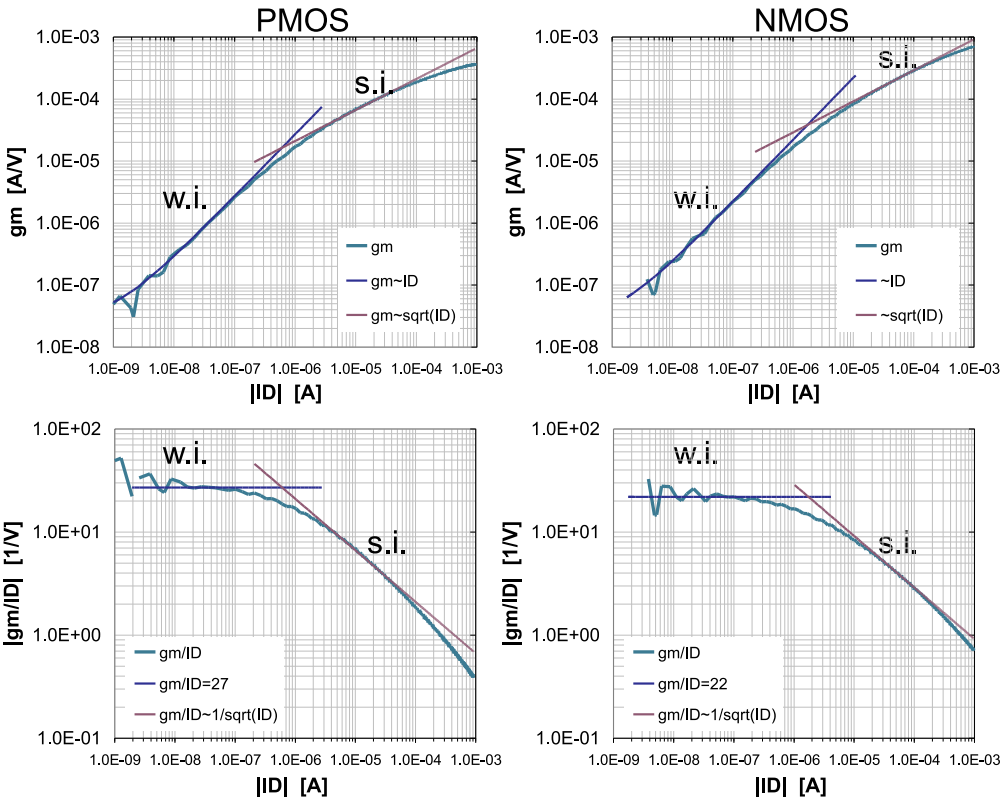


Figure 5.10: Transconductance g_m and transconductance-current ratio g_m/I_D for PMOS and NMOS transistors with dimensions of $W/L = 40\mu\text{m}/3\mu\text{m}$, operating at the saturation ($|V_{DS}| = 3.8$ V) and produced on the wafer PT249. w.i. and s.i. indicate weak and strong inversion, respectively.

transconductance curves, reflecting the transition from the weak to strong inversion, may be observed. As expected, the maximum transconductance-to-current ratios (27 V^{-1} for PMOS and 22 V^{-1} for NMOS) are achieved for the weak inversion. Following the theoretical formula 5.11, the transconductance-to-current ratios drop down for the drain currents higher than the transition currents. The ratios reach the values of 5 V^{-1} at I_D of 18 μA for PMOS and 34 μA for NMOS transistors.

The transistor output conductance versus the drain current, calculated from a derivative of the output characteristic, is illustrated in a bilogarithmic scale in figure 5.11. The results are presented for three different transistor sizes: $W/L = 40\mu\text{m}/3\mu\text{m}$, $20\mu\text{m}/10\mu\text{m}$, $40\mu\text{m}/20\mu\text{m}$. As given by equations 5.15 and 5.16, the output conductance increases with increasing values of the drain current for a fixed value of the drain-source voltage. The slope of the $g_{ds}(I_D)$ characteristic allows extracting the LAMBDA parameters for each size of the tested devices. Consequently, the value of the Early voltage can be calculated relying on the relation 5.17. Obtained results for typical transistors produced on the wafer PT249 are summarized in table 5.3.

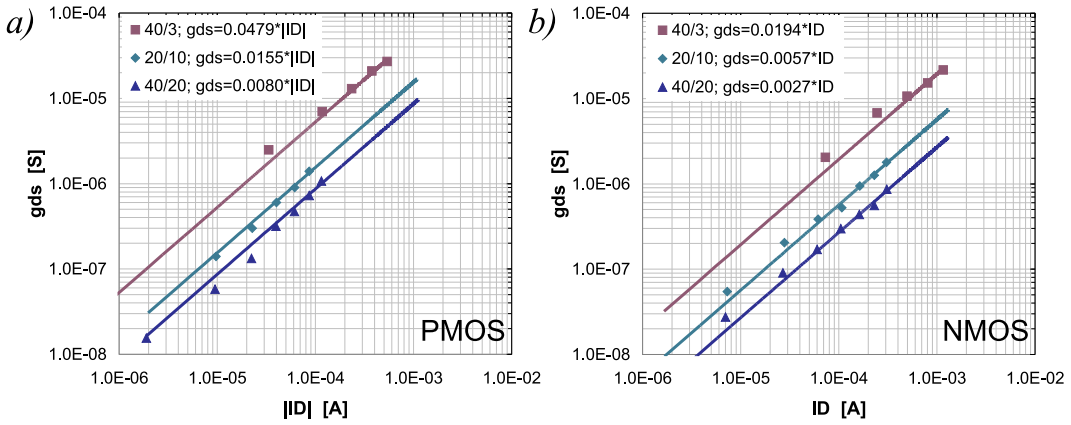


Figure 5.11: Output conductance g_{ds} versus drain current I_D for a) PMOS and b) NMOS transistors operating at the saturation (V_{DS} = 5 V). Results obtained for the transistors with dimensions of $W/L = 40\mu\text{m}/3\mu\text{m}$, $20\mu\text{m}/10\mu\text{m}$, $40\mu\text{m}/20\mu\text{m}$, produced on PT249.

The extracted values of the Early voltage for the PMOS and NMOS transistors are different due to the difference in the substrate doping for both types of devices. Since the lower the substrate doping is, the further the drain depletion layer extends toward the source, the channel length modulation is larger for the PMOS transistors than for the NMOS transistors manufactured in highly doped wells. Thus, at a given transistor operating point, the PMOS transistors have lower output resistance than the

Table 5.3: Extracted values of the LAMBDA and V_E parameters. Results obtained for typical transistors produced on wafer PT249 at $V_{BS} = 0\ V$ and $V_{DS} = 5\ V$.

	PMOS			**NMOS**		
$\frac{\mathbf{W}}{\mathbf{L}}\ [\frac{\mu\mathbf{m}}{\mu\mathbf{m}}]$	$\frac{\mathbf{40}}{\mathbf{3}}$	$\frac{\mathbf{20}}{\mathbf{10}}$	$\frac{\mathbf{40}}{\mathbf{20}}$	$\frac{\mathbf{40}}{\mathbf{3}}$	$\frac{\mathbf{20}}{\mathbf{10}}$	$\frac{\mathbf{40}}{\mathbf{20}}$
LAMBDA [1/V]	0.0479	0.0155	0.0080	0.0194	0.0057	0.0027
V_E [V/μm]	6.55			17.75		

NMOS transistors, which makes them less suitable for the design of current sources. As expected, lower values of the LAMBDA parameters were measured for the long channel transistors and for this reason, these devices should be used as active loads or current references in front-end electronics. The choice of the device dimensions has to be, however, a compromise between the circuit area and the performance.

The presented graphs of the transistor transconductance and the output conductance can be directly used as a reference in the design of the readout circuit. Relying on the characteristics presented in figures 5.10 and 5.11, the operating point for a particular architecture of the readout electronics may be chosen taking into account the requirements of the circuit bandwidth, noise and gain. Derived equations describing the transistor drain current at the saturation together with the extracted values of the n, K', LAMBDA and V_E parameters allow modelling the characteristics of the MOS devices produced in the SOI sensor technology without the knowledge of the exact values of the transistor Spice parameters.

Transistor leakage current

Next parameter, which was investigated for the new SOI technology, was the transistor leakage current. Usually, very low value of this parameter is required since it determines the static power consumption of digital circuits. As it will be presented in next chapter, the transistor leakage current may also cause parasitic discharging of an integrating capacitor and affect the value of the measured signal in the readout circuits operating in the charge integration mode.

The measurements of the leakage currents were performed for both PMOS and NMOS transistors with dimensions of $W/L = 6\mu$m$/3\mu$m and 40μm$/3\mu$m. During these tests, special care was taken to avoid influence of light on measurements results. Since very low values of the current signals had to be sampled, the integration time of the semiconductor parameter analyzer was extended to minimize noise and interferences.

Subthreshold characteristics obtained for the wafer PT249 are presented in figure 5.12. Acceptable leakage currents below a picoamp for the transistors with dimensions of $W/L = 6\mu\text{m}/3\mu\text{m}$ were measured at the drain-source voltage of 5 V and the temperature of 23°C. Relying on the characteristics obtained for different sizes of transistors, the following values of the I_{D0} parameter (present in equation 5.10) were also extracted:

$$I_{D0} = 0.225 \text{ pA} \quad \text{for PMOS}$$

$$I_{D0} = 0.080 \text{ pA} \quad \text{for NMOS}$$

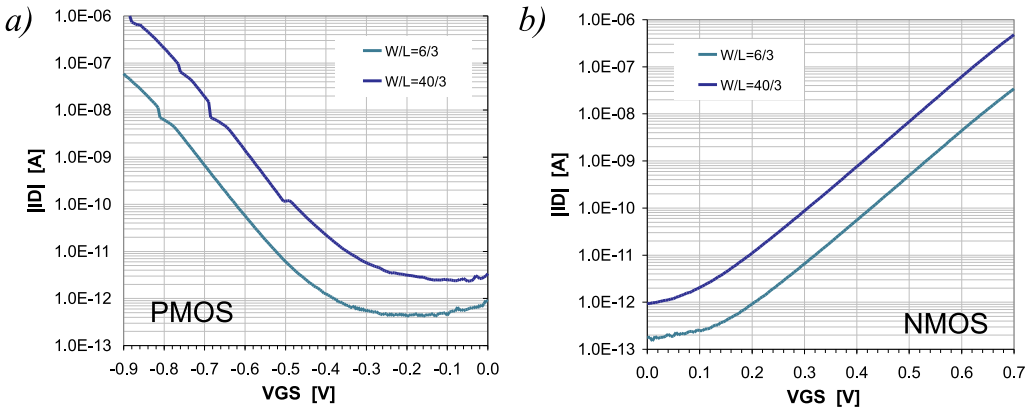


Figure 5.12: Typical subthreshold characteristics of a) PMOS and b) NMOS transistors with dimensions of $W/L = 6\mu\text{m}/3\mu\text{m}$ *and* $40\mu\text{m}/3\mu\text{m}$*, produced on PT249.*

Comparison of transistors from different lots

Last group of the transistor measurements was focused on the comparison of basic device parameters for different technological iterations. At early stage of the new SOI technology development (wafers PT29, PT28 and PT249), the main goal of such measurements was to find the technology revision that allows achieving desired readout electronics characteristics. Once the technological parameters had been adjusted, these measurements allowed controlling the reproducibility of the transistor characteristics for different lots (wafers PT249, PT229 and PT246).

The extracted values of the threshold voltages, the current factors, the substrate doping and the GAMMA and PHI parameters for different wafers are summarized in a chronological order in table 5.4. The values of the threshold voltage V_{T0} and the $\frac{K'}{2}\frac{W}{L}$ factor were obtained using the method illustrated in figure 5.7 at the zero bulk-source polarization, while the values of the GAMMA, PHI and NSUB factors were extracted from the equations 5.3, 5.4 and 5.5.

Table 5.4: Summary of basic transistor parameters for different wafers.

		PMOS			**NMOS**		
	$\frac{\mathbf{W}}{\mathbf{L}}$ $[\frac{\mu\mathbf{m}}{\mu\mathbf{m}}]$	$\frac{\mathbf{6}}{\mathbf{3}}$	$\frac{\mathbf{20}}{\mathbf{10}}$	$\frac{\mathbf{40}}{\mathbf{20}}$	$\frac{\mathbf{6}}{\mathbf{3}}$	$\frac{\mathbf{20}}{\mathbf{10}}$	$\frac{\mathbf{40}}{\mathbf{20}}$
PT29	V_{T0} [V]	-1.06 ±0.04	-1.11 ±0.02	-1.11 ±0.02	0.77 ±0.01	0.81 ±0.01	0.81 ±0.01
	$\frac{K'}{2}\frac{W}{L}$ $[\mu A/V^2]$	9.3 ±0.8	9.0 ±0.2	8.7 ±0.1	26.3 ±1.9	25.4 ±0.6	24.6 ±0.3
	GAMMA $[V^{0.5}]$	0.64			1.10		
	PHI [V]	0.64			0.69		
	NSUB $[cm^{-3}]$	3.5×10^{15}			10.3×10^{15}		
PT28	V_{T0} [V]	-0.95 ±0.01	-0.94 ±0.01	-0.95 ±0.01	0.90 ±0.01	0.93 ±0.01	0.94 ±0.01
	$\frac{K'}{2}\frac{W}{L}$ $[\mu A/V^2]$	7.5 ±0.4	8.8 ±0.1	8.8 ±0.1	19.9 ±0.7	23.3 ±0.3	23.1 ±0.2
	GAMMA $[V^{0.5}]$	0.64			1.11		
	PHI [V]	0.64			0.69		
	NSUB $[cm^{-3}]$	3.5×10^{15}			10.5×10^{15}		
PT249	V_{T0} [V]	-0.87 ±0.04	-0.87 ±0.04	-0.87 ±0.04	0.76 ±0.02	0.77 ±0.03	0.78 ±0.02
	$\frac{K'}{2}\frac{W}{L}$ $[\mu A/V^2]$	8.9 ±0.4	11.8 ±0.4	11.8 ±0.4	21.6 ±0.7	25.1 ±1.9	24.8 ±2.4
	GAMMA $[V^{0.5}]$	0.43			1.05		
	PHI [V]	0.60			0.69		
	NSUB $[cm^{-3}]$	1.6×10^{15}			9.4×10^{15}		
PT229	V_{T0} [V]	-0.68	-0.69	-0.71	0.72	0.74	0.74
	$\frac{K'}{2}\frac{W}{L}$ $[\mu A/V^2]$	11.2	13.1	12.9	26.0	27.6	28.0
	GAMMA $[V^{0.5}]$	0.32			0.96		
	PHI [V]	0.56			0.68		
	NSUB $[cm^{-3}]$	0.9×10^{15}			7.8×10^{15}		
PT246	V_{T0} [V]	-0.83	-0.83	-0.83	0.79	0.81	0.81
	$\frac{K'}{2}\frac{W}{L}$ $[\mu A/V^2]$	10.8	12.3	12.4	26.0	27.6	28.0
	GAMMA $[V^{0.5}]$	0.37			1.04		
	PHI [V]	0.58			0.69		
	NSUB $[cm^{-3}]$	1.2×10^{15}			9.2×10^{15}		

As presented in table 5.4, the first iteration of the SUCIMA1 test structure (wafer PT29) was characterized by asymmetric values of the threshold voltage. This asymmetry was especially dangerous in view of the character of damages that occur in transistors exposed to ionising radiation. As reported in [44], one of the main results of the radiation damages in MOS transistors is positive charge trapping in the gate oxide. This translates into decrease of the threshold voltage of NMOS transistors and increase of the absolute value of the threshold voltage of PMOS transistors. Thus, the observed asymmetry of the V_{T0} parameter before irradiation would become even more significant after the transistor operation in radiation environment. It might lead to permanent switching-on of the NMOS devices and cutting-off the PMOS ones. For this reason, the phosphorus doping dose used for the compensation of the initial p-type film into n-type was decreased during processing of the wafer PT28. In such a way, lower absolute values of the V_{T0} parameter were achieved for the PMOS transistors and higher values – for the NMOS transistors.

Starting from the wafer PT249 the test structures were produced on the Analog Devices substrates, which resulted in the modification of transistor parameters. In particular, the bulk doping concentration of the PMOS transistors decreased by a factor of two with reference to the SOITEC wafers (PT29 and PT28). Consequently, it translated into the change of the threshold voltages and other doping depended parameters, such as the GAMMA and PHI factors. The effect of the decrease of substrate doping concentration for the PMOS transistors may be also observed in figure 5.8, where the comparison of the body effect characteristics for the wafers PT28 and PT249 is depicted. Despite some changes of the device characteristics, the set of parameters obtained for the PMOS and NMOS transistors produced on the wafer PT249 was considered to be satisfactory and was used as a reference for next technological runs.

Although no significant changes were introduced into CMOS components processing in later lots (i.e. wafers PT229 and PT246), table 5.4 shows further variations of the transistor parameters. The comparison of the values of the GAMMA and PHI factors indicates that the parameters spread results from differences of the body and well doping concentrations. Since the measured values of the substrate doping concentration change in the same direction for both types of transistors (for example NSUB decreases for both PMOS and NMOS transistors on PT229), it may be expected that this effect derives from the absolute thickness variations of the silicon film of the AD wafers.

Larger standard deviations of parameters of the transistors coming from the same wafer are also noticeable for the devices produced on the Analog Devices substrates. For example, table 5.4 indicates that the threshold voltage mismatches increase from 1.1 % to 4.6 % for the PMOS transistors manufactured on the wafers PT28 and PT249, respectively. As presented in figure 5.8, the variations of the threshold voltages on th wafer PT249 become even more significant for non-zero body-source voltages, which points at non-uniformity of the silicon film thickness within a wafer and, consequently, non-uniformity of the doping concentration of the transistor bulk.

Observed for the AD wafers variations of the device layer thickness are ascribed to the applied method of the thin film formation. As mentioned, these wafers are thinned down using mechanical grinding and polishing. The silicon surface uniformity guaranteed by the foundry admits thickness variations of 200 % for the nominal film thickness in the SOI detector. Thus, worse matching and larger global parameters variations of the transistor produced on the AD wafers are unavoidable and has to be controlled.

Current Mirrors Unit

Current mirror unit is another structure of the SUCIMA1 and SUCIMA2 test chips, which allows investigations of technological parameters variations [85] of the new SOI technology. The schematic view and the layout of this unit is presented in figure 5.13. The test circuit consists of a wide set of NMOS and PMOS current mirrors with dimensions of W/L [μm/μm]: 7.5/3, 15/3, 10/10, 12.5/10, 25/10, 50/10, 100/10, 25/20 and 50/20. All the transistors have the same layout and orientation. Transistors with dimensions of 50μm/10μm and 15μm/3μm are repeated (in direct proximity) three times on every test structure so the matching characteristics of the neighbouring current mirrors along with the global parameters variations may be studied.

The evaluation of the spread of transistor parameters in this unit is performed by the comparison of the output currents I_{OUT} of the current sources with nominally exactly the same dimensions. The measurements may be performed for two types of input signals: a current signal injected into the drain of the input transistor (W/L = 100μm/10μm) or a voltage signal applied between the common gate and source contacts of a transistors set. When the first type of the input signal is used, some of the global parameters variations between different test chips on a wafer are compensated. For example, if the typical value of the threshold voltage at certain

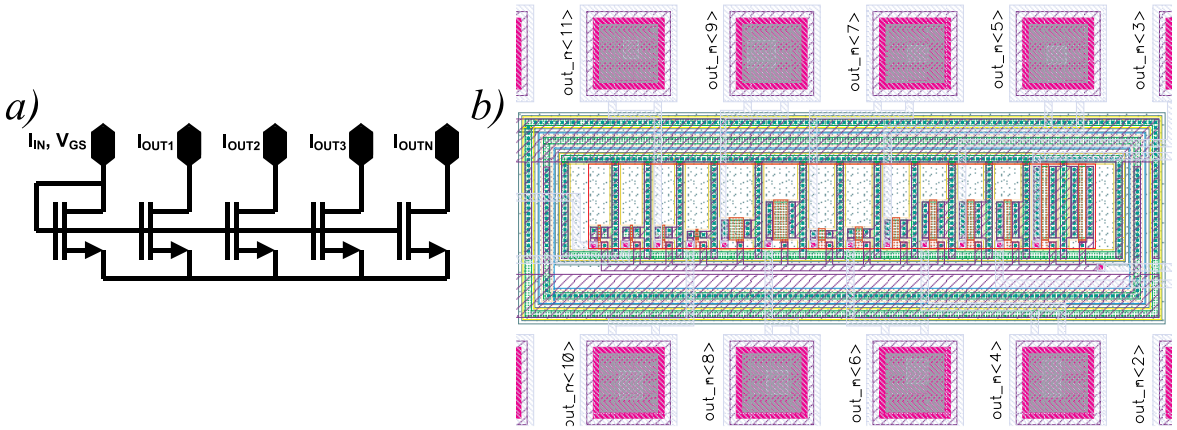


Figure 5.13: a) Schematic view and b) layout of the current mirrors unit.

area of the wafer is increased, it will affect in the same way the injection and tested transistors. Therefore, the voltage signal is more suitable for studying the global parameters variations.

The output signal variation obtained with the current mirrors unit is a superposition of the mismatches of several MOS transistor parameters, i.e. the process current factor K', the device dimensions W/L and the threshold voltage V_{T0}. Mismatches of these parameters result from the variations of other physical quantities, such as: the gate oxide thickness and the mobility in the case of the process current factor, and the gate oxide thickness and the substrate doping in the case of the threshold voltage [84, 86]. In general, the relation between the output current spread and the variations of the threshold voltage and the current factor can be expressed by the following formula:

$$\frac{\sigma^2(I_{OUT})}{I_{OUT}^2} = \frac{\sigma^2\left(K'\frac{W}{L}\right)}{\left(K'\frac{W}{L}\right)^2} + 4\frac{\sigma^2(V_{T0})}{(V_{GS}-V_{T0})^2} \tag{5.18}$$

where $\sigma(I_{OUT})$ is measured standard deviation of the output current, while $\sigma(K'\frac{W}{L})$ and $\sigma(V_{T0})$ are standard deviations of the $K'\frac{W}{L}$ product and the threshold voltage, respectively.

The characteristics of the $\frac{\sigma(I_{OUT})}{I_{OUT}}$ versus the gate-source voltage V_{GS}, measured for the devices produced in the new SOI sensor technology, are shown in figure 5.14. The results are presented for various current source dimensions and wafers. Each curve in figure 5.14 represents global parameter variations over a wafer. As expected from

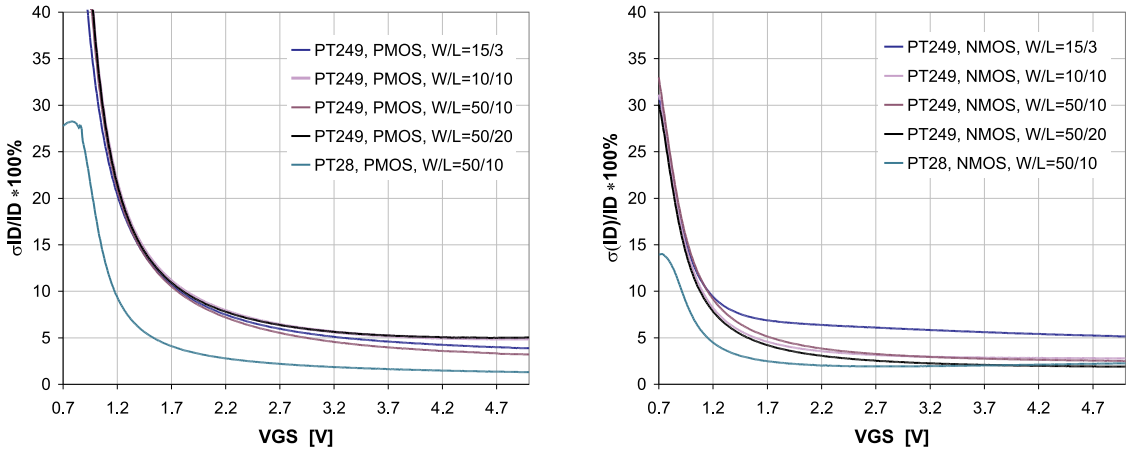


Figure 5.14: Measured characteristics of $\frac{\sigma(I_{OUT})}{I_{OUT}}$ *versus* V_{GS} *voltage for various current source dimensions and wafers.*

formula 5.18, the most significant current variations are observed for the low and moderate inversions. The characteristics of the $\frac{\sigma(I_{OUT})}{I_{OUT}}$ saturate for high values of the gate-source voltage V_{GS}. This indicates that for $V_{GS} \gg V_{T0}$, the first factor in equation 5.18 is dominating:

$$\frac{\sigma\left(K'\frac{W}{L}\right)}{K'\frac{W}{L}} \approx \left.\frac{\sigma(I_{OUT})}{I_{OUT}}\right|_{V_{GS}\gg V_{T0}} \tag{5.19}$$

Taking into account the above relation and fitting the measured characteristics of the output current variations, the values of $\frac{\sigma\left(K'\frac{W}{L}\right)}{K'\frac{W}{L}}$ and $\sigma(V_{T0})$ can be roughly estimated. The results are summarized in table 5.5. As presented, larger parameters mismatches (especially in the case of PMOS transistors) are obtained for the lot produced on the grinded wafer (PT249) than on the implant enhanced split wafer (PT28). For the NMOS devices, the process current variations are almost in inverse proportion to the square root of the device area, while for the PMOS devices no particular dependence on the transistor dimensions is observed. For both types of transistors, the technological parameters variations obtained with the considered current source unit are in fine agreement with the results obtained by direct measurements of the transistor threshold voltage and the current factor.

Table 5.5: Global relative variations of transistor parameters measured with the use of the current sources unit of the SUCIMA1 test structure. Results measured for the devices coming from the same wafer.

	PMOS					**NMOS**				
	PT249				**PT28**	**PT249**				**PT28**
$\frac{\mathbf{W}}{\mathbf{L}}$ $[\frac{\mu\mathbf{m}}{\mu\mathbf{m}}]$	$\frac{\mathbf{15}}{\mathbf{3}}$	$\frac{\mathbf{10}}{\mathbf{10}}$	$\frac{\mathbf{50}}{\mathbf{10}}$	$\frac{\mathbf{50}}{\mathbf{20}}$	$\frac{\mathbf{50}}{\mathbf{10}}$	$\frac{\mathbf{15}}{\mathbf{3}}$	$\frac{\mathbf{10}}{\mathbf{10}}$	$\frac{\mathbf{50}}{\mathbf{10}}$	$\frac{\mathbf{50}}{\mathbf{20}}$	$\frac{\mathbf{50}}{\mathbf{10}}$
$\frac{\sigma\left(K'\frac{W}{L}\right)}{K'\frac{W}{L}} \cdot 100\%$	3.2	4.3	2.5	4.6	1.1	5.3	2.7	2.4	1.8	2.0
$\sigma(V_{T0})$ [mV]	48	44	45	41	15	19	17	21	17	6

Complementary measurements of local matching properties of the current mirrors were performed by a current injection into the input transistor of every mirrors set. Due to the small quantity of the current sources laid in direct proximity, the local mismatches $\frac{\Delta I_{OUT}{}^{(I_{IN},\ loc)}}{I_{OUT}{}^{(I_{IN},\ loc)}}$ were expressed by the average relative difference of the measured value and the local mean value of the output current. The results are summarized in table 5.6. As presented, comparable matching properties of the current mirrors produced on both tested wafers were measured. These results indicate that the developed technology is characterized by satisfactory local matching properties even at low currents. Nevertheless, the global parameters variations can be critical in the case of the MOS transistors produced on the substrates thinned down by mechanical grinding and polishing.

Table 5.6: Local matching properties of current sources.

		PMOS				**NMOS**			
$\frac{\mathbf{W}}{\mathbf{L}}$ $[\frac{\mu\mathbf{m}}{\mu\mathbf{m}}]$		$\frac{\mathbf{50}}{\mathbf{10}}$		$\frac{\mathbf{15}}{\mathbf{3}}$		$\frac{\mathbf{50}}{\mathbf{10}}$		$\frac{\mathbf{15}}{\mathbf{3}}$	
$\mathbf{I_{IN}}$ [μA]		10	50	10	50	10	50	10	50
$\frac{\Delta I_{OUT}{}^{(I_{IN},\ loc)}}{I_{OUT}{}^{(I_{IN},\ loc)}}$ ·100%	PT28	0.5	0.4	3.5	2.5	0.6	0.3	2.3	1.4
	PT249	1.0	0.6	2.7	1.8	0.5	0.4	2.1	1.6

Capacitors Unit

In previous paragraphs, characteristics and mismatches of such basic elements of integrated circuits as transistors were examined. Other important devices of electronic circuits are capacitors. The mismatches of these components were investigated in the test structure illustrated in figure 5.15. In this structure, the relative difference between capacitance values of two nominally the same capacitors C_X and C_Y is obtained by

measurements of the transfer characteristic of the presented circuit for two connection configurations – pad X connected to the voltage signal source and pad Y grounded, and vice versa. From the slope of these two transfer characteristics (S_X and S_Y, respectively) the capacitors mismatches and the ratio of the capacitance values C_X and C_Y may be calculated in the fallowing way:

$$\frac{\Delta C}{C} = 2\frac{C_X - C_Y}{C_X + C_Y} = 2\frac{S_X - S_Y}{S_X + S_Y} \tag{5.20}$$

$$\frac{C_X}{C_Y} = \frac{S_X}{S_Y} \tag{5.21}$$

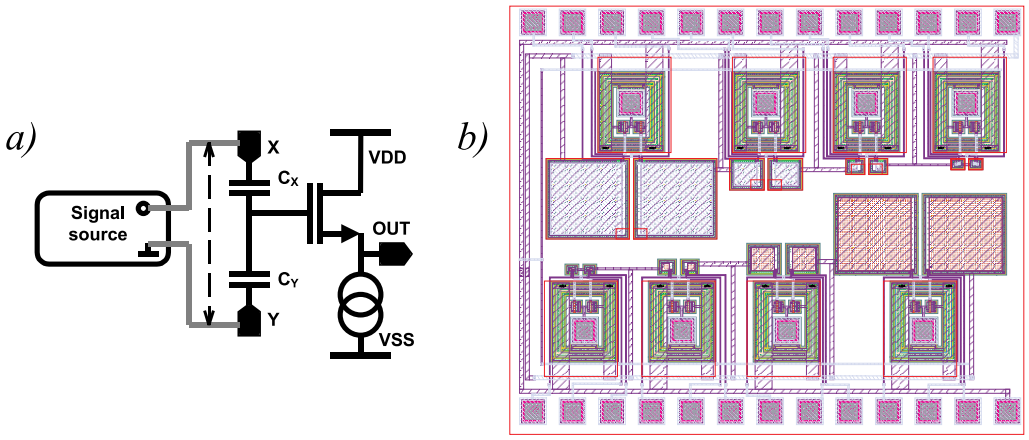


Figure 5.15: Capacitors mismatches measurements: a) the connection diagram and b) the layout of the test structure.

The measurements were performed for three different capacitance values (about 100 fF, 1pF and 10 pF) and for two capacitors types: polysilicon – metalization level 1 and metalization level 1 – metalization level 2. The typical mismatch $\frac{\Delta C}{C}$ was calculated as the average relative mismatch obtained for the particular couples of capacitors. As presented in table 5.7, satisfactory matching properties were measured even for small capacitance values (around 2% for 100 fF capacitor). No significant differences in the matching characteristics for both kinds of the capacitors were also observed.

Table 5.7: Results of the mismatches measurements for poly-Si - metal 1 and metal 1 - metal 2 capacitors with different dimensions (and values).

	PolySi – Metal 1			**Metal 1 - Metal 2**		
C [pF]	≈ 0.04	≈ 0.4	≈ 4	≈ 0.07	≈ 0.7	≈ 7
$\mathbf{W}\times\mathbf{L}$ [μm$\times\mu$m]	37×37	117×117	370×370	37×37	117×117	370×370
$\frac{\Delta C}{C}\cdot 100\%$	1.70	1.18	0.34	2.03	1.42	0.22

Simple analogue circuits

Another part of the SUCIMA1 test structure includes samples of such analogue circuits as amplifying stages in common source (OS) and common source – common gate (OS-OG) configurations. The schematics of these circuits are presented in figure 5.16. The main purpose of the design of these elements was examination of the DC characteristics and the performance of circuits manufactured in miscellaneous revisions of the new technology. In addition, the comparison of the measurements and the simulations of these circuits played an important role in the verification of the quality of the MOS transistor Spice models provided by the foundry.

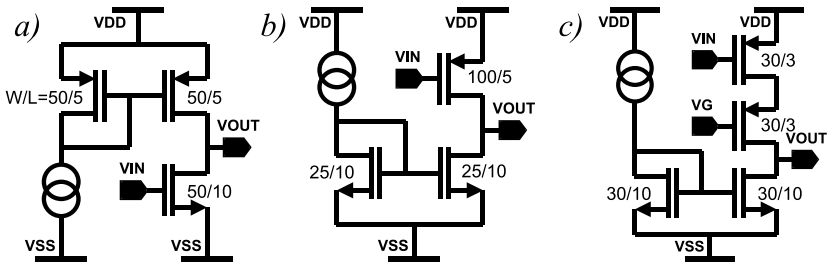


Figure 5.16: Schematic views of basic amplifying stages: a) a common source configuration with NMOS input transistor, b) a common source configuration with PMOS input transistor and c) a common source - common gate configuration.

Examples of the measured transfer and gain versus bias current characteristics for the common source and common source - common gate amplifiers produced on the wafers PT29, PT28 and PT249 are presented in figures 5.17-5.19. As illustrated, despite some changes in the DC characteristics, all the technology versions offer similar performance of the amplifying stages for the investigated moderate and strong

inversions. In agreement with equations 5.11 and 5.15, decrease of the aplifiers gain with the square root of the bias current I_{BIAS} was also measured for the strong inversion.

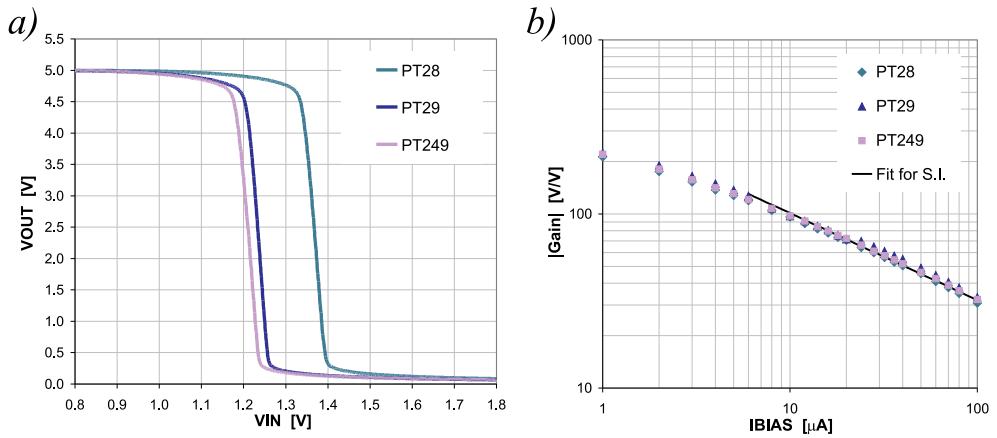


Figure 5.17: Measurements results of the OS amplifiers with NMOS input transistors produced in different technology iterations: a) transfer characteristics at the bias current of 10 µA, b) gain versus bias current in a bilogarithmic scale.

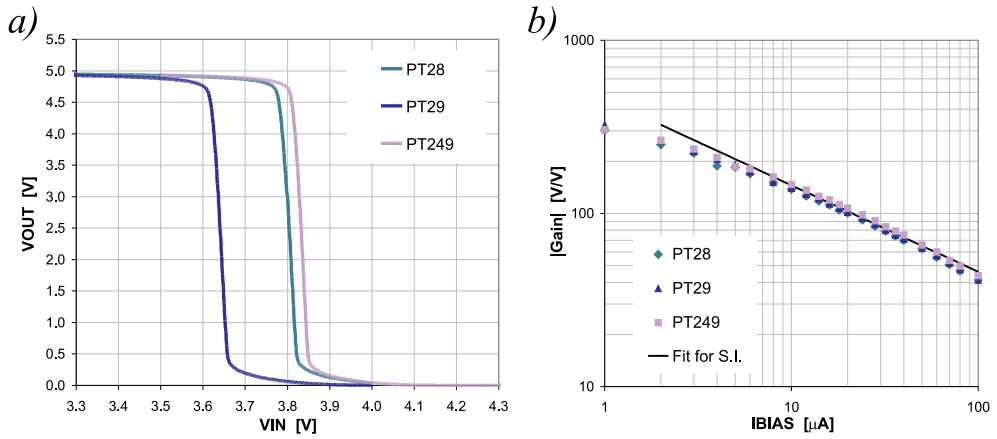


Figure 5.18: Measurements results of the OS amplifiers with PMOS input transistors produced in different technology iterations: a) transfer characteristics at the bias current of 10 µA, b) gain versus bias current in a bilogarithmic scale.

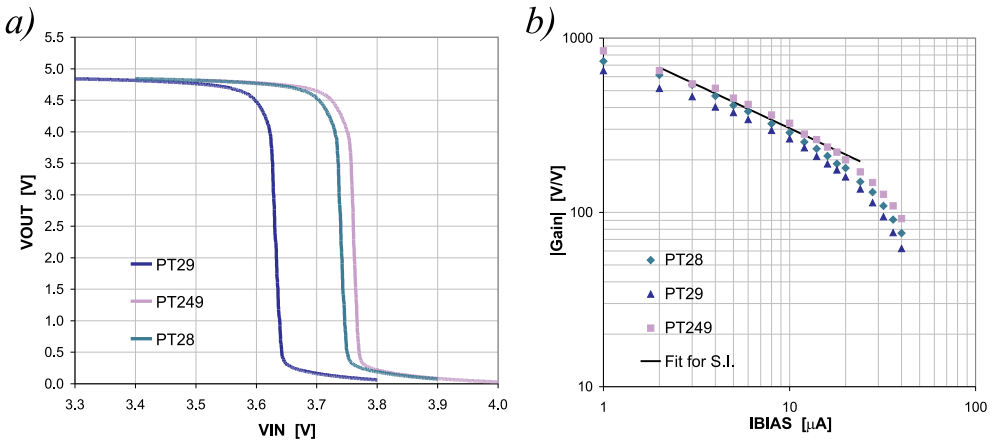


Figure 5.19: Measurements results of the OS-OG amplifiers produced in different technology iterations: a) transfer characteristics at the bias current of 10 μA, b) gain versus bias current in a bilogarithmic scale.

The characteristics measured for the amplifiers manufactured on the wafer PT249 were also juxtaposed with the results obtained by simulations and simplified calculations based on equations 5.11 and 5.15. Models level 3 provided by IET were used for the simulations, while the parameters given in tables 5.3 and 5.4 were exploited for the hand calculations. The comparison of the results obtained for the OS amplifiers is given in figure 5.20. As presented, the simulated gain versus current characteristics

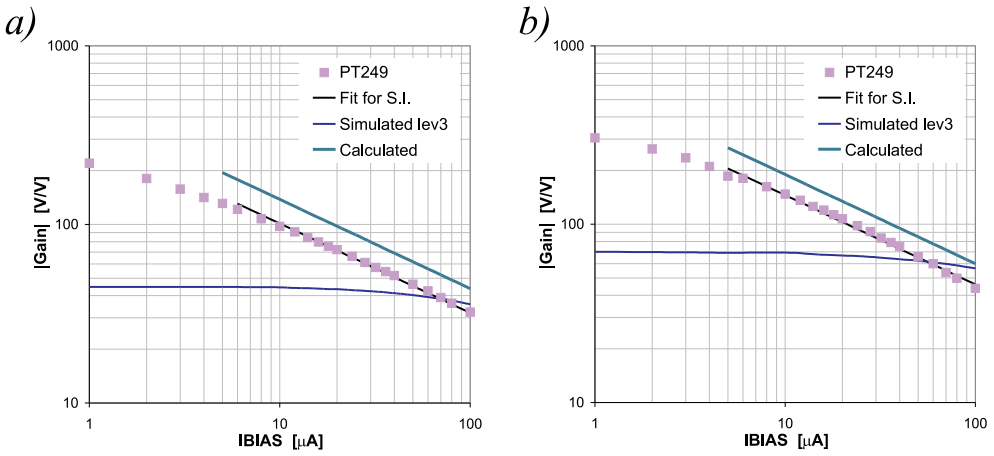


Figure 5.20: Comparison of the measured and simulated gain versus bias current characteristics for the OS amplifiers with a) NMOS and b) PMOS input devices.

differ to a large extend from the experimental results. This is mainly related to inaccurate modelling of the slope of the output characteristics of PMOS devices. The hand calculations also lead to slight overestimation of the gain value, but the character of the gain changes as a function of bias current I_{BIAS} is modelled better. Obtained results indicate that simplified empirical model proposed in one of the previous paragraphs can be used for the calculations of small signal parameters with satisfactory accuracy.

Simple digital circuits

Apart of the simple amplifying stages, the SUCIMA1 test structure containes also some basic digital circuits. These circuits constituted an origin of a library of standard digital cells required for the design of digital blocks of SOI sensor prototypes. The basic library consisted of the following cells: standard inverter INV1, double load inverter INV2, double load buffer BU2, NAND gate, NOR gate and data flip-flop with asynchronous reset DFA. Like other elements of the SUCIMA1 chip, the dimensions of the transistors building the digital cells were chosen relying on the simulation results obtained with the device models for the standard CMOS technology. These dimensions were subsequently adjusted according to the measurements results. The layouts of the initial digital circuits are presented in figure 5.21.

The measurements of the digital cells designed on the SUCIMA1 and SUCIMA2 test structures consisted of several stages. First, general logical tests of these circuits were performed. For all the digital cells, reliable functionality was proofed at the nominal supply voltage of 5V, the low input signal levels from 0 to 0.5 V and the high input signal levels from 4.5 to 5 V. After these basic tests, the transfer characteristics of the digital gates were measured. The results obtained for different technology versions are presented in figure 5.22. For all the technological lots, some asymmetry of the transfer characteristics was observed as the result of the difference of the carriers mobility in the bulk transistors models and the mobility obtained on the SOI wafers. To avoid such an asymmetry in next lots, the dimensions of the NMOS transistors in the digital gates and the data flip-flop were increased.

At last, the dynamic parameters of the digital gates produced in the IET-SOI technology were evaluated. Since test circuits for the measurements of dynamic parameters were not designed on the SUCIMA1 chip, the propagation delays and the rise/fall times were measured only for the standard inverter taking advantage of

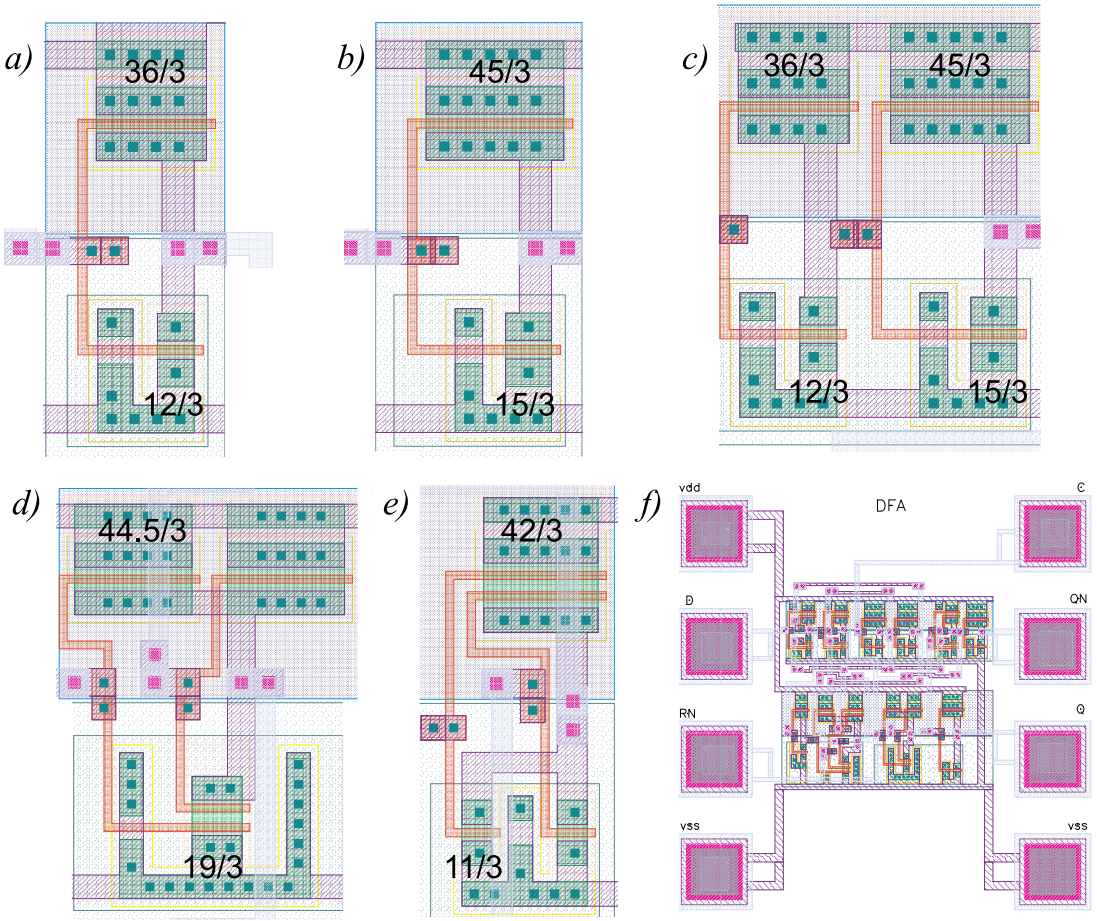


Figure 5.21: Layouts of digital cells: a) inverter, b) double load inverter, c) buffer, d) NAND gate, e) NOR gate and f) data flip-flop.

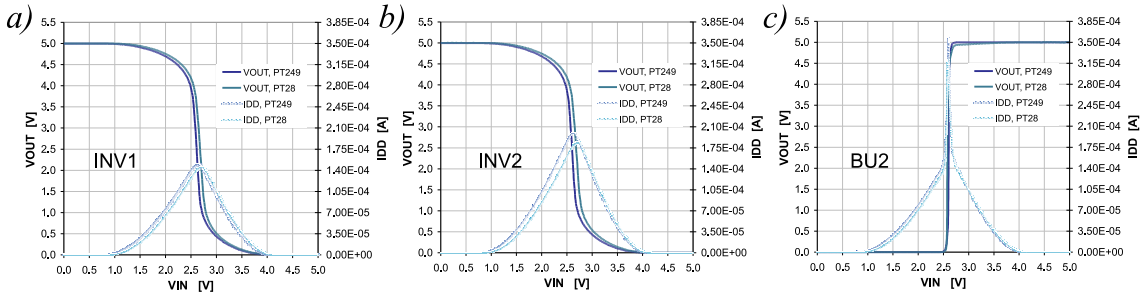


Figure 5.22: Output voltage and supply currents versus input voltage for selected digital gates produced on the wafers PT28 and PT249: a) standard inverter, b) double load inverter and c) double load buffer.

the fact that the buffer cell (depicted in figure 5.23) is a two-stage circuit consisting of a standard inverter and a double load inverter. In order to measure the parameters of this gate, the INV2 and BU2 gates were assembled on a printed circuit board and the circuits responses for the signals from a pulse generator were observed with the oscilloscope probes directly connected to the gates outputs. In such a way, rise, fall and propagation times of the INV2 and BU2 cells loaded by bonding pad and oscilloscope probe capacitances were measured. These values were subsequently used to calculate the dynamic parameters of the standard inverter loaded by a double load inverter. The following values of the rise time t_r, the fall time t_f, the high-to-low propagation delay t_{pHL} and the low-to-high propagation delay t_{pLH} were obtained:

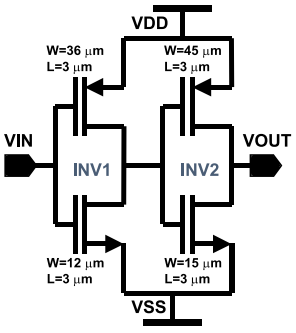
$$t_r = 34 \text{ ns}$$

$$t_f = 43 \text{ ns}$$

$$t_{pHL} = 11 \text{ ns}$$

$$t_{pLH} = 10 \text{ ns}$$

The above values should allow the operation of the digital circuits with frequencies up to few MHz for relatively short chains (up to about 10) of gates. To allow proper operation for a larger number of cascaded gates or higher load capacitances, double load or additionally designed fourfold load gates (INV4 and BU4) have to be used in the design of control blocks of the SOI sensor prototypes.



$$t_{pHL,LH}(INV1) \approx t_{pHL,LH}(BU2) - t_{pHL,LH}(INV2)$$

$$t_{r,f}(INV1) \approx \sqrt{t_{r,f}^2(BU2) - t_{r,f}^2(INV2)}$$

Figure 5.23: Schematic view of the buffer cell and the calculation method of dynamic parameters of the inverter cell.

5.3.2 Characterization of Detector Junctions

As mentioned, the most specific aspect of the SOI sensor technology is the presence of such non-CMOS components as detector junctions produced below the buried oxide layer. For this reason, the SUCIMA1 and SUCIMA2 test chips contain special modules required for the characterization of the quality of the pixel p-n junctions and the examination of the integration reliability of the radiation sensitive and front-end parts of the monolithic sensor. In the case of the SUCIMA1 chip, these modules are a part of the technological test structure designed at the Institute of Electron Technology. They include two reliability test structures: a chain of 100 contact windows to pixel diodes and a metalization level 1 serpentine over 100 deep detector contact windows, as well as a test structure for the measurements of the detector I-V characteristics. The latest consists of 3 detector diodes with dimensions of W/L = 105 μm x 105 μm and 21 μm x 525 μm. On the contrary to the standard diodes designed in the way illustrated in figure 5.2, one of the pixel diodes of the test structure is not protected by a polysilicon ring around the junction contact. Microscopic photographs of the described test structures are presented in figure 5.24.

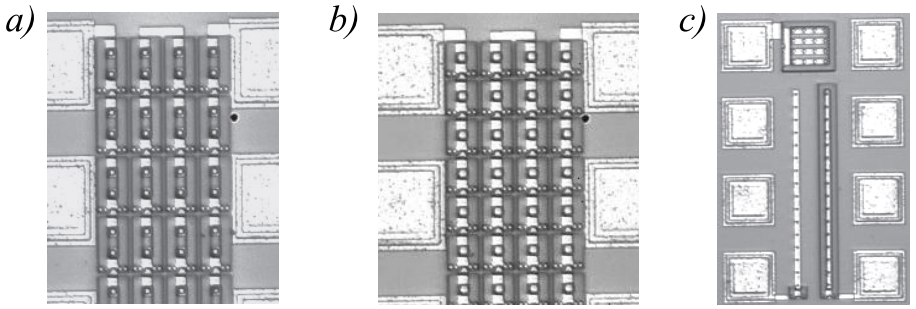


Figure 5.24: Microscopic photos of the test stuctures dedicated to the SOI sensor application and designed on the SUCIMA1 test chip - fragments of the reliability test structures: a) a chain of contact windows to the pixels and b) a metal serpentine over pixel cavities, c) a test structure for the measurements of pixels junctions parameters - detector diodes with dimensions of W/L = 105 μm x 105 μm and 21 μm x 525 μm.

The disadvantage of the test structure designed on the SUCIMA1 chip is the fact that the depleted volume cannot be unambiguously defined when the reverse bias voltage is applied to the detector backplane. Though the thickness of the active volume is limited by the sensor thickness, the lateral extension of the depleted zone in this test structure depends on the resistivity of the detector material, which may vary

from one wafer to another. Therefore, another module for the measurements of the I-V and C-V characteristics of detector junctions was designed on the SUCIMA2 test chip. The proposed test structure consists of 2 matrices of 10 by 10 bare detector diodes with the pixel pitch of 150 μm and 80 μm. The matrices are surrounded by a single or double detector guardring in the form of a continuous p^+ implantation in the detector substrate. The main purposes of the guardrings are limiting the electric field expansion in the lateral direction in the detector substrate and isolating the detector active volume from other modules produced on the wafer. The pixels of the matrices are collected into several sets in order to limit the number of the test points. Internal pixels of the matrices are grouped into four sets of 16 pixels each, while external pixel form a separate set of 36 pixels. This allows assessing the effectiveness of the guardring structure by comparing leakage currents of the pixels located in the middle of the matrix and at its peripheries. At last, a contact to the upper silicon layer is placed among detector diodes to enable investigation of the influence of the electronics substrate polarization on the detector performance. The layout of the designed test structure is presented in figure 5.25.

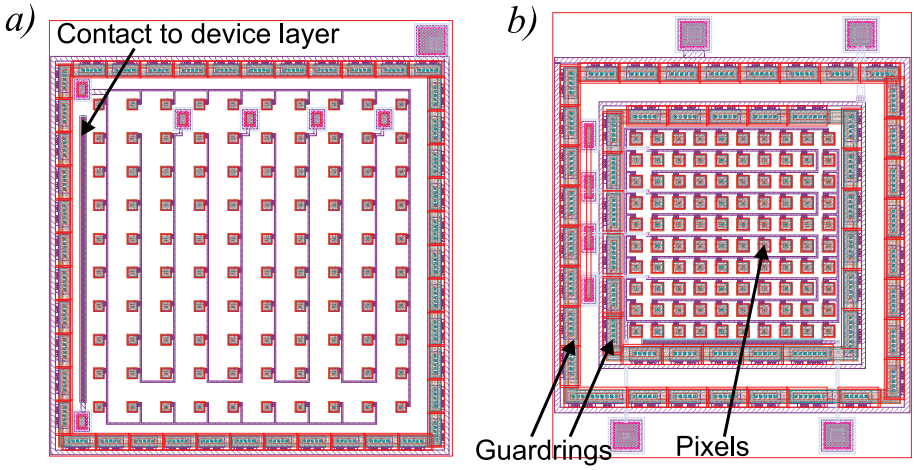


Figure 5.25: Layout of the test stucture dedicated to the I-V and C-V characteristics measurements of the pixel diodes of the SOI sensor - matrices of 10 by 10 bare detector diodes with the pixel pitch of a) 150 µm and b) 80 µm. Test structures designed on the SUCIMA2 test chip.

As the first step of the quality verification of the pixel construction, the reliability tests of the structures designed on the SUCIMA1 chip were performed. The measurements performed at the IET indicated proper connections to the detector junctions and continuous electrical paths above pixel cavities for almost 100 % of the tested structures [82].

The quality of the detector junctions was assessed by the measurements of the reverse characteristics of the test pixels on the SUCIMA1 test structure. The measurements performed for the first lot of the SUCIMA1 chip indicated heterogeneity and relatively high values of the measured leakage currents. About 39 % of the square pixels on the wafer PT249 exhibited proper operation for the investigated range of the detector bias voltage V_{DET} up to 100 V, but about 43 % of the pixels had the breakdown voltages close to the full depletion voltage (40-70 V). The remaining square pixels were characterized by extremely high leakage currents even at low detector bias voltage. Similar results were obtained for the rectangular pixels with the standard construction and other wafers from the first lot of the SUCIMA1 test chip. Exemplary reverse characteristics and the complete distributions of the leakage currents obtained on the wafer PT249 at room temperature are presented in figures 5.26 and 5.27. The results are also compared with those obtained on the best of the processed wafers, indicated by PT234. As illustrated, the leakage currents of order of $2 - 20 \times 10^{-10}$ and 8×10^{-11} per diode with dimensions of 105 μm x 105 μm were measured at the bias voltage of 60 V for good pixels on PT249 and PT234, respectively. Assuming the impurities concentration in the detector substrate in the range of $4 - 11 \times 10^{11}\mathrm{cm}^{-3}$, the given values correspond to the normalized leakage currents of a few dozen to a few hundred nanoamps pre square centimetre for the first lot of the SUCIMA1 test structures and of a few to a few dozen of nanoamps pre square centimetre for the best wafer. Obtained results show significant improvement in the uniformity of the junction quality and lower values of the leakage currents on the wafer PT234.

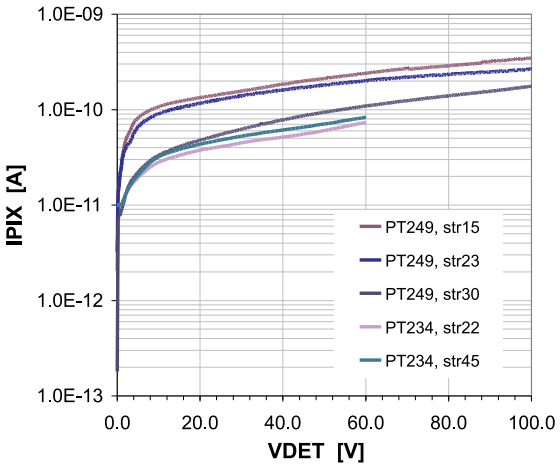


Figure 5.26: Leakage current I_{PIX} versus detector bias voltage V_{DET} per pixel with dimensions of 105 μm x 105 μm. Results presented for the best pixels on the wafers PT249 and PT234. Results for the wafer PT234 are presented with the IET consent.

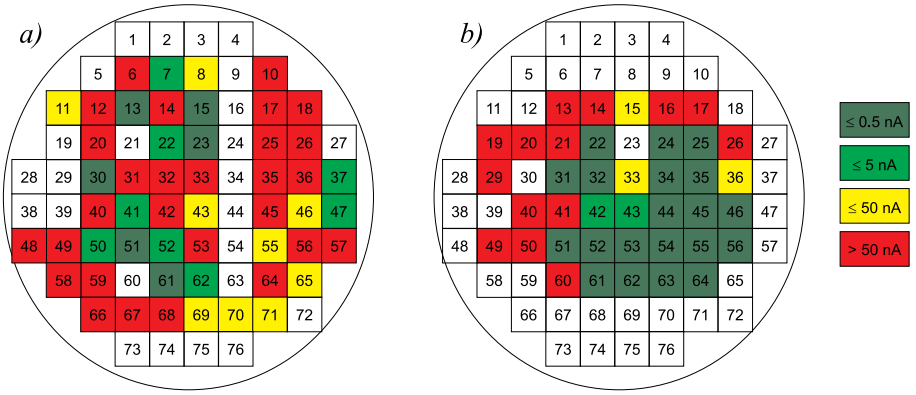


Figure 5.27: Distributions of the leakage current per pixel at the bias voltage of 60 V and at room temperature: a) wafer PT249, b) wafer PT234.

The measurements of the SUCIMA1 test structures were also used for the optimisation of the formation method of the detector junctions. The effectiveness of preventing the pixel implantations from contamination with the use of a polysilicon barrier was investigated by the comparison of the reverse characteristics obtained for the rectangular pixels with and without a polysilicon ring. Almost all the pixels without the polysilicon barrier exhibited low breakdown voltages (below 45 V), which may suggest the necessity of the protection of the detector substrate below the pixel openings. For further protection of the high resistivity material, IET proposed also additional technological steps for preventing the detector backplane from unintentional scraping and contamination. As reported in [75], using thick oxide layer at the detector backside during the technological sequence allowed reducing pixel leakage currents by several orders of magnitude in comparison with the reference wafers produced without such a protection. A number of technological experiments was also performed at the foundry to study the dependence of the detector junction quality on the doping method of the pixel. In particular, the pixel formation by the implantations of B-11, BF_2, F+B-11 and the diffusion from a boron-doped amorphous silicon layer were examined. The best results were achieved for the low-dose implantation of B-11 [75].

The measurements described above allowed preliminary definition of the manufacturing technology of the SOI sensor. After this development stage, the SUCIMA2 test structure was produced and characterized. This chip was fabricated together with first real-size prototypes of the SOI sensors. As the sensor prototypes occupied most of the wafer area, only two pieces of the SUCIMA2 test structure were available on every examined wafer.

The measurements of the SUCIMA2 structure produced on the wafers PT229 and PT246 indicated extremely high leakage currents (of order of dozens of microapms per square centimeter). Most of the tested chips exhibited the breakdown voltages below 100 V, too. Exemplary I-V characteristics obtained for the matrices of pixel diodes (figure 5.25) are given in figure 5.28. As presented, despite the efforts towards improving the sensor technology, unsatisfactory quality of the detector junctions was observed. This effect may be partially ascribed to the fact that the structures were produced on the edges of the wafers. As it will be presented in chapter 6, other measurements performed for a large-scale detector prototype indicated the normalized leakage currents of 290 nA per square centimetre for the best sensor. This value is still higher than expected for good silicon particle detectors.

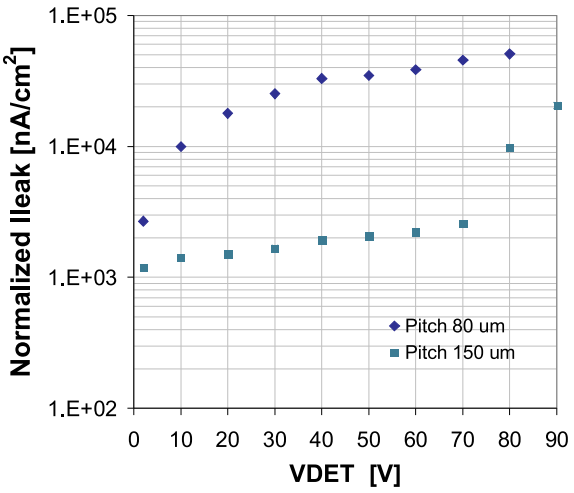


Figure 5.28: Normalized leakage current of the pixel diodes versus detector bias voltage V_{DET}. Results obtained for the matrices with the pixel pitch of 80 μm and 150 μm produced on the wafer PT229.

In order to determine if the origin of the poor detector performance lies in the processing steps or the quality of the starting material, the generation lifetime for the AD wafers was measured at the foundry. A relatively low value of 200 μs was obtained. According to the equation 2.18, the measured generation lifetime translates into the generation currents around 500 nA/cm^2 for 400 μm thick detector. This result indicates that the quality of the starting material has a significant effect on the parameters of the new sensor. Although the destructive effect of the sensor processing steps on the

performance of the charge sensitive part of the new monolithic pixel sensor cannot be excluded, some improvement of the quality is expected for better SOI wafers. This statement has not been confirmed experimentally because the adequate research is still carried on.

The test structures presented in figure 5.25 were also exploited for the examination of the capacitance versus voltage characteristics of the pixel junctions produced together with the large-scale prototypes of the SOI sensors. Before the tests, the I-V characteristics were probed to exclude the structures with the breakdown voltage below 90 V. The C-V characteristics were measured with the use of the Quadtech LCR meter and an external high voltage source. The open and short circuit calibrations of the system were performed before each measurement, but the value of the parasitic capacitance of a connection pad and a metal line was not compensated.

The measured C-V characteristics are presented in figure 5.29. In order to extract the value of the full depletion voltage, the results are presented as the inverted square value of the measured capacitance versus the reverse bias voltage. As illustrated, the full depletion voltage of approximately 40 V can be found for the matrix with the pitch of 80 μm. The full depletion voltage of the larger structure is not apparent.

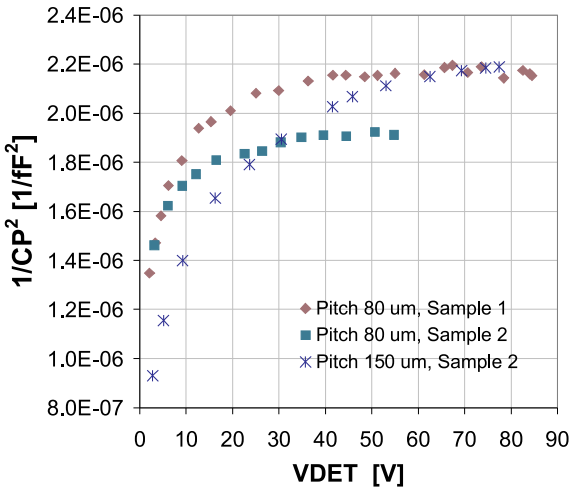


Figure 5.29: C-V characteristics of the pixel diodes obtained for the matrices with the pixel pitch of 80 μm and 150 μm produced on the wafer PT229.

The structures designed on the SUCIMA2 test chip allowed also tracing an important fault of the SOI detector technology. As the matrices presented in figure 5.25 have an additional contact to the device layer, the sensor active substrate and

the electronics bulk could be biased simultaneously. Such an experiment revealed local short circuits between the pixel diodes and the device layer. This problem was extensively examined and it was concluded that the most probable source of this fault is a defect in the insulating layer between the polysilicon barrier covering the pixel cavity and the device layer. As the polysilicon coat is connected to the metal line leading to the detector diode in all the existing prototypes of the SOI sensor, such a defect translates into the short circuit between the mentioned metal line and the pixel implantation. To overcome this problem, excluding the polysilicon barrier in the future prototypes of the SOI sensor was proposed by the Institute of Electron Technology. Since the polysilicon layer played an important role in the proposed structure of the SOI sensor, some technological experiments aiming at the investigation the reliability of the connection and the quality of the sensitive junctions had to be performed for the modified technology. As presented in figure 5.30, the continuity of a metal path led directly over 5 μm deep cavity in bulk silicon was confirmed. As the previous measurements showed much worse performance for the detector diodes without the polysilicon coat, the leakage currents and the breakdown voltages for the sensors produced in the revised process have to be still assessed.

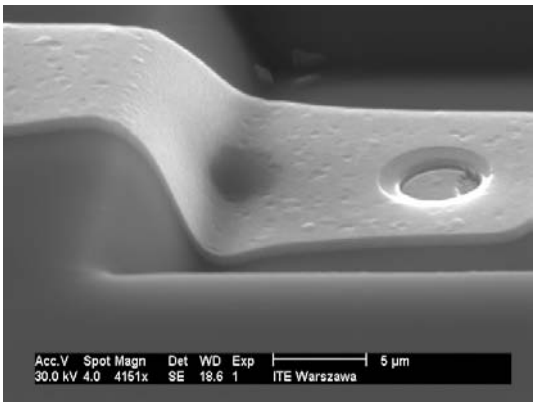


Figure 5.30: Microscopic photograph of a metal path led directly over a 5 μm thick cavity etched down in bulk silicon (presented with the IET consent).

An alternative solution of the problem of the short circuit between the polysilicon coat covering the pixel cavity and the device layer is connecting the coat to the supply line instead of connecting it to the input of the readout circuit [87]. If the polysilicon layer and the electronics substrate are connected to the same potential, the short circuit between them does not affect the sensor operation. In contrast to the

approach proposed by the IET, such a solution does not require any modification of the technology, though it consumes slightly larger area of the readout cell. The advantage of both solutions in comparison with the conventional structure of the cavity of the SOI sensor (illustrated in figure 5.2) is larger flexibility in the optimization of the capacitance seen from the input of the readout channel. As it will be discussed later, it plays an important role in increasing the sensor sensitivity to minimum ionising particles or low energy X-rays.

Chapter 6

SOI Detector Prototypes

The measurements results presented in previous chapter allowed setting-up the SOI sensor technology and evaluating the performance of basic components of the SOI sensor, such as pixel diodes and MOS transistors. The feasibility of the complete sensor had to be still investigated. Although basic physics of the device could be verified by simulations, it was expected that the quality of the buried oxide and the handle wafer of an SOI substrate might be crucial for the sensor performance. For this reason, a series of small and large-scale SOI sensor prototypes were designed and manufactured. Due to the complexity of the SOI sensor technology, very simple test structures, consisting of 64 detector cells, were designed and extensively tested as a first step of the verification process [82, 88, 89, 90]. Once the general concept of the sensor was validated, large-scale, completely functional SOI sensors were developed [89, 91, 92]. These sensors consisted of more than 16 thousands channels and according to the requirements of the SUCIMA project [9], they were optimized for medical imaging applications. The design and the measurements results obtained for both test structures and real-size SOI sensors will be addressed in this chapter.

6.1 SOI Sensor Test Structures

6.1.1 Design of SOI Sensor Test Structures

First test structures of the monolithic active pixel sensors realized in SOI technology were manufactured as units of the SUCIMA1 test chip. At the time when the SUCIMA1 chip was designed, the IET-SOI technology was at an early stage of the development and the design rules for the pixel formation and the model files for electronic circuit

simulations did not exist. Therefore, the sensor test structures were designed in very simple forms of small matrices of pixel diodes connected to readout channels. Digital control blocks and an analogue output buffer were not implemented on the chip to allow free access to the particular channels of the test sensors and to give flexibility of the choice of the readout sequence.

Apart of the matrices of complete SOI sensor cells, matrices of bare readout channels with input pads in the place of the detector diodes were proposed to asses the characteristics of the readout electronics itself. This way, eventual problems with MOS devices in the readout channels could be easily distinguished from the performance of the radiation sensitive part of the sensor.

A block diagram of the SOI sensor test structure is presented in figure 6.1. The matrices of the complete test sensors consist of 8 by 8 readout cells, while the matrices of the bare front-end electronics consist of 5 by 5 or 5 by 6 readout cells, depending on the circuit version. The schematic views of the readout channels implemented on the test structures are presented in figure 6.2. Both presented configurations have the structure similar to the typical three transistor cell (3T), mentioned in chapter 3. The main element of such a readout cell is the input transistor M1 in the common drain configuration, which separates the detector diode from the output node. During the channel readout, which is initiated by switching on the row selection transistors (Mrow or Mrow_a and Mrow_b) and column selection transistors (located outside the active matrix), the M1 transistor is connected to the current source (common for the readout matrix) and the recorded signal is transferred to the output. The value of the output voltage signal is determined by the gain of the source follower and the capacitance value at the input node. This capacitance constitutes the charge integrating element of the readout cell and it may be discharged by switching on the reset transistor M2 in order to begin a new charge integration cycle.

Since the SOI approach allows using NMOS and PMOS transistors in a sensor cell, some modifications are made in the design of the readout channel to enhance its performance. In particular, the reset transistors of the opposite type than the input transistors are used to achieve faster discharging of the integrating capacitances and, in the case of the configuration presented in figure 6.2-b, the single-transistor channel selection switches are replaced by transmission gates to obtain better linearity and dynamic range.

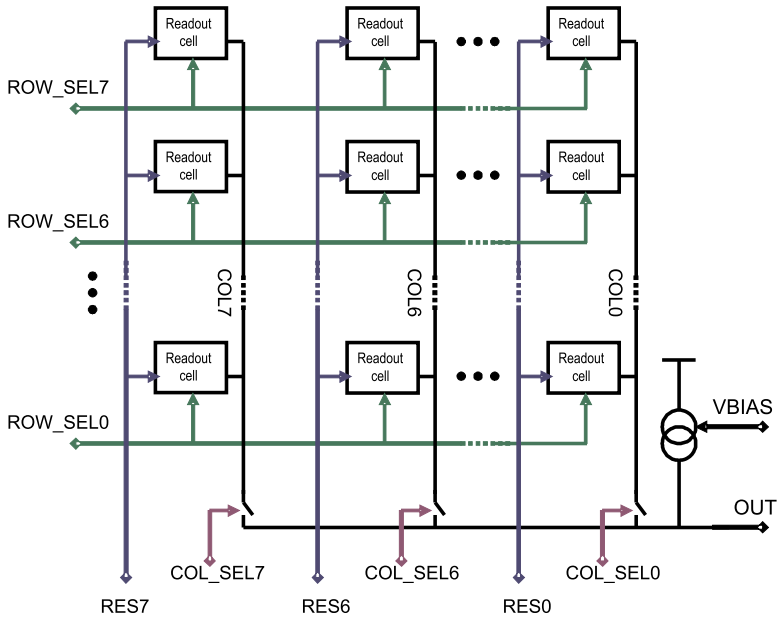


Figure 6.1: Block diagram of the SOI sensor test structure.

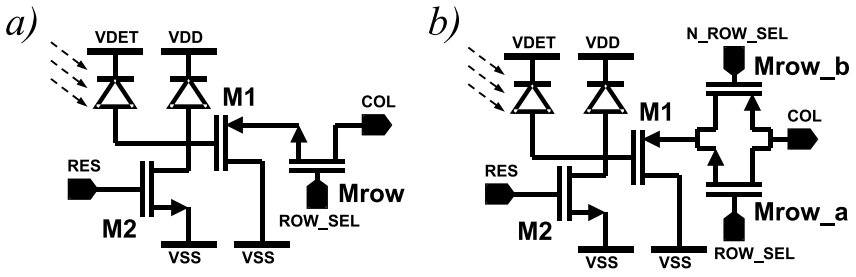


Figure 6.2: Readout cell of the SOI sensor: a) with a single-transistor row-selection switch, b) with a row-selection switch in the form of a transmision gate.

The beneficial effect of the use of the reset transistor of the opposite type than the input transistor on the reset dynamics is explained in figure 6.3. If the input and reset transistors are of the same type (as in the standard 3T cell illustrated in figure 3.3-b), the gate-source voltage of the reset transistor decreases as the voltage on the integrating capacitance drops off due to discharging. Therefore, the operating point of the reset transistor changes in the way illustrated by turquoise plot in figure 6.3-a. The drain current decreases quickly and the reset transistor enters the week inversion for low voltages on the integrating capacitance. On the other hand, if the input and reset transistors are of the opposite type, the latter transistor operates at constant

gate-source voltage (of 5 V) and its drain current during the reset is much higher than in the previous case. As the result, the time required to remove the charge collected on the integrating capacitance is much shorter, which is illustrated in figure 6.3-b.

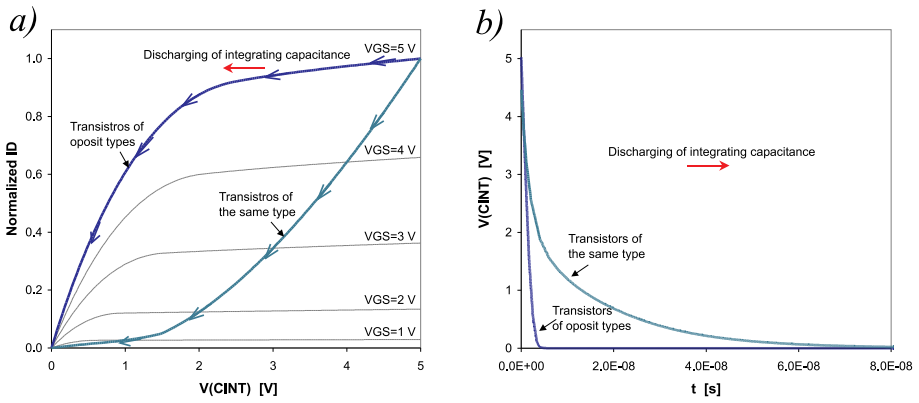


Figure 6.3: Illustration of the beneficial effect of using the reset transistor of the opposite type than input transistor: a) changes of the operating point of the reset transistor during discharging of the integrating capacitance C_{int}, b) voltage on the integrating capacitance during reset. V(CINT) indicates the voltage on the integrating capacitance. Exemplary characteristics presented for $C_{int} = 200\ fF$ and NMOS reset transistor with W/L=3.

Apart of the mentioned above modifications of the basic 3T cell, the readout channel configuration for the SOI sensor is distinguished by the presence of an additional reverse biased diode between the channel input and the positive supply voltage VDD. This diode is realized as a P-well-N-substrate structure and acts as an input protection circuit. Such a protection is required due to the DC coupling between the readout channels and the detector diodes and due to the high bias voltage applied to the backplane of the SOI sensor. During the sensor operation, the pixel leakage current together with the signal generated by traversing particles causes increase of the potential level at the input of the readout cell. As the detector can be biased with high voltages, uncontrolled raise of the potential at the input might destroy the readout channel. This is prevented by switching-on the protecting diode once the voltage at the input of the transistor M1 exceeds the positive supply voltage. Of course, the protecting diode contributes also to the dark current of the sensor. Nevertheless, performed measurements indicated that the reverse current of the P-well-N-substrate diode is negligible in comparison with the leakage current of the pixel diodes of the SOI sensor.

The layouts of the designed cells with integrated pixel diodes are presented in figure 6.4. The dimensions of the cells are 140 μm x 122 μm for the channel configuration with a single-transistor switch (figure 6.2-a) and 140 μm x 140 μm for the channel configuration with a transmission gate (figure 6.2-b). The main elements of the readout cells can be distinguished on the layouts. All the active devices of the sensor cell are surrounded by a guardring in the form of n^+ diffusion connected to the supply voltage. The guardring ensures good electronics polarization and reduces the cross-talk between neighbouring channels. In the left upper corners of the layouts, connections to the pixel diodes are visible. As presented, the polysilicon ring around the pixel is connected to the input of the readout circuit, which prevents from building up fixed charge in the polysilicon layer. In order to ensure continuity of the electrical path in the pixel cavity, a large plate of metalization covers the walls of the cavity over the polysilicon layer. Since this plate is short-circuited with the polysilicon ring, it does not add any additional capacitance at the input node. The main component of the readout cell is the input transistor with dimensions of W/L = 40μm/3μm. Apart of these basic elements of the SOI readout channel, an additional capacitor in the form of a polysilicon-metal1 plate is added in parallel with the input of the readout cell in order to optimize the sensor for the high flux of particles expected for the beam monitor application [9, 13].

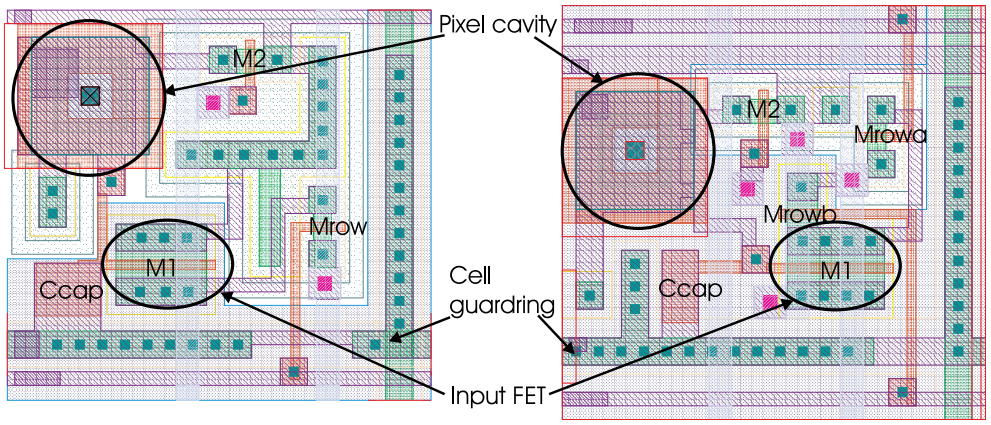


Figure 6.4: Layouts of the cells of the SOI sensor test structures: a) channel configuration with a single-transistor switch and b) channel configuration with a transmission gate.

6.1.2 Evaluation of Charge-to-Voltage Conversion Gain

The SOI sensor cell described above operates in the charge integration mode, which means that the value of the output signal is proportional to the charge generated in the sensor active volume and integrated during a given time period (integration time t_{int}) on a charge integrating capacitance C_{int}. The relation between the amplitude of the output signal V_{OUT} and the collected charge Q_{coll} is called charge-to-voltage gain $G_{Q\rightarrow V}$. It is defined as:

$$G_{Q\rightarrow V} = \frac{dV_{OUT}}{dQ_{coll}} \tag{6.1}$$

and it is typically expressed in mV/fC. Alternatively, the charge-to-voltage gain may be referred to the number of the collected charge carriers N_q:

$$G_{N_q\rightarrow V} = qG_{Q\rightarrow V} = \frac{dV_{OUT}}{dN_q} \tag{6.2}$$

and then it is expressed in μV/e$^-$.

In the case of the SOI sensor test structure, the charge-to-voltage gain is given by:

$$G_{Q\rightarrow V} = k_{u0}\frac{1}{C_{int}} \tag{6.3}$$

The k_{u0} parameter in the above equation is the low frequency gain of the source follower. It can be calculated from the model of the readout circuit and the small signal model of the source follower presented in figures 6.5 and 6.6, respectively. Taking into account that:

$$V_{gs} = V_{in} - V_{out} \qquad \text{and} \qquad V_{bs} = -V_{out}$$

the general formula describing the gain of the source follower is derived:

$$k_u(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1} + sC_{gs1}}{g_{m1} + g_{mb1} + g_{ds} + s(C_{gs1} + C_{pl})} \tag{6.4}$$

where g_{m1} and g_{mb1} are the transconductance and the bulk transconductance of the transistor M1, $g_{ds} = g_{ds1} + g_{ds3}$ is a sum of the output conductances of the transistors M1 and M3, C_{gs1} is the gate-source capacitance of M1 and $C_{pl} = C_{pcol} + C_L$ is the parasitic capacitance of a column line, an output line, an output pad and the input of an external amplifier. C_{pl} dominates the capacitance between the output of the source follower and the ground. Above equation translates into the following form of the low frequency gain of the source follower:

$$k_{u0} = \frac{g_{m1}}{g_{m1} + g_{mb1} + g_{ds}} \tag{6.5}$$

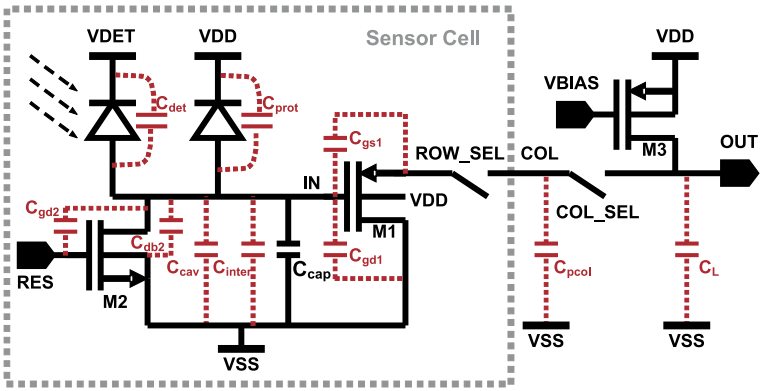


Figure 6.5: Schematic view of the readout circuit of the SOI sensor with marked parasitic capacitances required for the calculation of the charge-to-voltage gain.

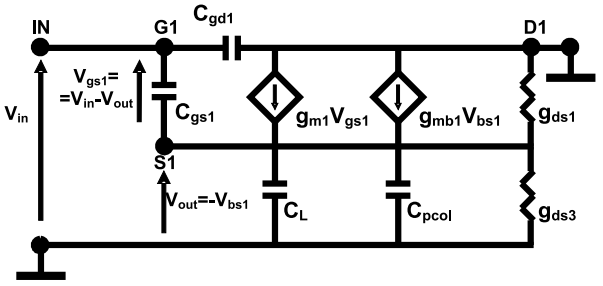


Figure 6.6: Small signal model of a source follower.

The values of the transconductance g_{m1} and the output conductance g_{ds}, required for the gain calculation, can be found in figures 5.11 and 5.10. Assuming the drain current of the source follower of $I_D = 20\ \mu$A, one obtains:

$$g_{m1} = 95\ \mu\text{S} \qquad\qquad g_{ds} = 1\ \mu\text{S}$$

Since the output conductance is nearly two orders lower than the transconductance, it can be neglected. The remaining quantity - bulk transconductance of the transistor M1 - is a function of the transconductance and the bulk-source voltage V_{BS} of the transistor M1. It is expressed as [93]:

$$g_{mb1} = \frac{\text{GAMMA}}{2\sqrt{|\text{PHI}| + |V_{BS}|}}\, g_{m1} = \eta g_{m1} \tag{6.6}$$

After putting the above equation into 6.5, the following formula for the low frequency gain k_{u0} of the source follower is obtained:

$$k_{u0} \approx \frac{1}{1+\eta} \tag{6.7}$$

As the η parameter in equation 6.7 depends on the bulk-source voltage of the transistor M1, k_{u0} depends on the output voltage. However, it is more convenient to express it as a function of the voltage at the input node. As presented in figure 6.5, the bulk-source voltage of the transistor M1 is equal to:

$$V_{BS} = \text{VDD} - (V_{IN} + |V_{GS1}|)$$

where VDD is the positive power supply (typically VDD=5 V for the SOI sensor), V_{IN} is the voltage level at the input node IN and V_{GS1} is the gate-source voltage of the transistor M1 at its operating point. According to plot 5.9, $V_{GS1} \approx 1.2$ V for $I_D = 20$ μA. The value of the low frequency gain of the source follower as a function of the input voltage is illustrated in figure 6.7. The results are obtained taking into account the values of the GAMMA and PHI parameters extracted for the PMOS transistors produced on the reference wafer PT249 (table 5.4). As presented, the voltage-dependent character of the follower gain is one of the origins of the readout circuit non-linearity. For the input voltage range from 0 V to 3.5 V, the value of the low frequency gain may change by 5.35 % with reference to the middle value of:

$$k_{u0} = 0.86 \text{ V/V}$$

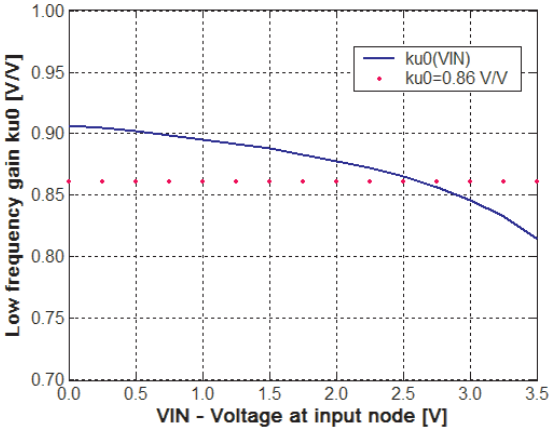


Figure 6.7: Low frequency gain of the source follower as a function of the voltage at the input node.

Second parameter that is required for the charge-to-voltage gain calibration is the integrating capacitance C_{int}. In order to calculate the value of this parameter, the capacitance seen from the input of the readout channel has to be found. As presented in figure 6.5, this capacitance has several components, which are related to:

- Capacitance of the additional capacitor increasing the dynamic range of the sensor C_{cap}
- Junction capacitance of the pixel diode C_{det}
- Junction capacitance of the protection diode C_{prot}
- Input capacitance of the source follower C_{insf}
- Capacitances associated with the drain of the reset transistor M2 C_{res}
- Parasitic capacitance of the polysilicon coat covering the walls of the pixel cavity C_{cav}
- Parasitic capacitance of the interconnection between the pixel diode and the readout channel input C_{inter}

Most of the values of these parameters can be only estimated. The calculation precision of the above capacitances depends on the accuracy of technological parameters provided by the foundry and may be not satisfactory for the new technology of the SOI sensor. In particular, the parasitic capacitance of the polysilicon plate in the pixel cavity cannot be precisely determined because the shape of the cavity as well as the thickness of the dielectric layer in the cavity are not well defined. Moreover, the shape of the cavity varies due to the non-uniformity of the device layer thickness, demonstrated in earlier measurements. This is expected to be one of the sources of the charge-to-voltage gain variations in the SOI sensors.

Apart of the uncertainty and the variations of technological parameters, the origin of the input capacitance ambiguity is the voltage-depended character of junction capacitances. Although the junction capacitance of the pixel diode may be treated as a constant value for the detector bias voltage at least several volts higher than the full depletion voltage, the junction capacitances of the protection diode and the transistors are modified by an increase of the input voltage. It is also worth to point out that the shapes of capacitance-versus-voltage (C-V) characteristics of these capacitances are not easy to predict due to the presence of the buried oxide layer. Thus, the capacitance of the protection diode and transistor junctions can be only estimated with the use of conventional bulk models.

Although the value of the charge integrating capacitance cannot be precisely calculated, it has to be estimated to enable cross-check with experimental results, evaluate the non-linearity of the charge-to-voltage gain and investigate possible variations of the gain. The total integrating capacitance and its particular contributions can be calculated relying on the technological parameters provided by the Institute of Electron Technology and the sensor cell layout.

The values of the C_{cap} and C_{inter} capacitances are obtained straightforward from the area and the perimeter of the additional capacitor and the interconnection lines, respectively. In a similar way, the parasitic capacitance C_{cav} is evaluated, but in this case, the V-shape of the pixel cavity must be taken into account. The area of the polysilicon coat may be divided into the flat part outside the etching region and the sloping part inside the pixel cavity. To calculate the latter contribution, the geometry presented in figure 6.8-a may be used. As presented, the device layer thickness is parameterized in order to investigate the result of the device layer non-uniformity on the value of the integrating capacitance.

A more complex task is the calculation of the capacitive contributions introduced by the transistors building the readout channel. As mentioned, these contributions are related to the input capacitance of the source follower and the terminal capacitances associated with the drain of the reset transistor M2. According to the small signal model 6.6, the input capacitance of the source follower is given by:

$$C_{insf} = C_{gd1} + (1 - k_{u0})C_{gs1} \tag{6.8}$$

where C_{gd1} and C_{gs1} are the gate-drain and gate-source capacitances of the input transistor M1 and k_{u0} is the follower gain given by 6.5 and 6.7. The gate-drain C_{gd} and gate-source C_{gs} capacitances are related to the gate-channel capacitance and the gate-source/drain overlap capacitances resulting from the lateral diffusion of the source and the drain underneath the polysilicon gate. The values of these capacitances depend on the operating point and for the saturation region, they are typically modelled by:

$$C_{gd} = \mathrm{CGDO} \cdot W \tag{6.9}$$

$$C_{gs} = \mathrm{CGSO} \cdot W + \frac{2}{3} C_{ox} \cdot LW \tag{6.10}$$

where CGSO and CGDO are the Spice parameters describing the overlap capacitances per channel width and $C_{ox} = 5.31 \times 10^{-16}$ F/μm^2 is the gate oxide capacitance per unit area.

The terminal capacitances associated with the drain of the reset transistor M2 include the gate-drain capacitance C_{gd2} and the bulk-drain capacitance C_{bd2}. Since the reset transistor is cut-off during the integration time, the C_{gd2} capacitance is formed by the gate-drain overlap capacitance and it is expressed by equation 6.9. In turn, the C_{bd2} capacitance is the junction capacitance of the reverse biased drain-bulk junction. In the standard bulk model, it is represented by the sum of a bottom plate junction capacitance and a sidewall junction capacitance. The first component is described by CJ - zero-bias junction capacitance per unit area and MJ - bulk-junction grading coefficient, while the second component is described by CJSW - zero-bias sidewall capacitance and MJSW - sidewall grading coefficient. The bulk-drain capacitance is voltage dependent and it is given by:

$$C_{bd} = \mathrm{AD}\frac{\mathrm{CJ}}{\left(1+\left|\frac{V_R}{\mathrm{PB}}\right|\right)^{\mathrm{MJ}}} + \mathrm{PD}\frac{\mathrm{CJSW}}{\left(1+\left|\frac{V_R}{\mathrm{PB}}\right|\right)^{\mathrm{MJSW}}} \tag{6.11}$$

where V_R is the reverse bias voltage, AD and PD are the area and the perimeter of the drain diffusion and PB is the bulk junction potential. The same formula describes the junction capacitance of the protection diode. In this case, the set of the Spice model parameters (CJ, MJ, CJSW, MJSW and PB) suitable for the P-well-to-N-substrate junction and the dimensions of the protection diode have to be used.

The capacitance of the pixel diode can be estimated assuming the full depletion of the detector substrate. The collecting junction may be modelled as a capacitor constituted by parallel plates with the area of a single sensor cell and the thickness equal to the total thickness of the radiation sensitive substrate (400 μm).

The calculated values of the particular contributions to the integrating capacitance C_{int}, obtained for the device layer thickness of 1.5 μm and the input voltage of 0 V, are summarized in table 6.1. The dependences of the charge integrating capacitance on the device layer thickness and the input voltage level are illustrated in figures 6.8-b and 6.8-c, respectively. As presented, the value of the integrating capacitance is mainly determined by the parasitic capacitance of the polysilicon coat covering the pixel cavity C_{cav} and the capacitances introduced by the transistors of the readout electronics (C_{insf} and C_{res}). The latter is dominated by the bulk-drain capacitance of the reset transistor (C_{bd2}). Due to the operation at full-depletion and the thick detector substrate, the contribution of the pixel diode (C_{det}) to the total capacitance seen at the input node is practically negligible.

Table 6.1: Contributions of the particular capacitances to the total integrating capacitance seen at the input node of a cell of the SOI sensor test structure. The values of the junction capacitances are calculated for zero voltage at the input node.

	C_{cap}	C_{det}	C_{prot}	C_{insf}	C_{res}	C_{cav}	C_{inter}
Area [μm^2]	385	17080	459	-	-	1061	-
Value [fF]	11.0	4.5	24.6	29.4	67.6	104.5	21.7

As presented in figure 6.8-b, the value of the integrating capacitance varies with the changes of the device layer thickness. Assuming the tolerance of the device layer thickness declared by the wafer manufacturer (± 0.5 μm), the parasitic capacitance of the polysilicon coat over the pixel cavity changes by ± 28.8 fF, which results in the relative variations of the integrating capacitance of 11 %. However, it does not take into account the influence of the device layer thickness on the junction capacitances and the technological parameters variations of all the components of the integrating capacitance. Due to the voltage-dependent character of junction capacitances, the value of the integrating capacitance depends also on the voltage level at the input node. Since the bulk-drain capacitance of the transistor M2 is connected between the input and the negative power supply, while the protection diode capacitance is connected between the input and the positive power supply, the value of C_{bd2} decreases and the

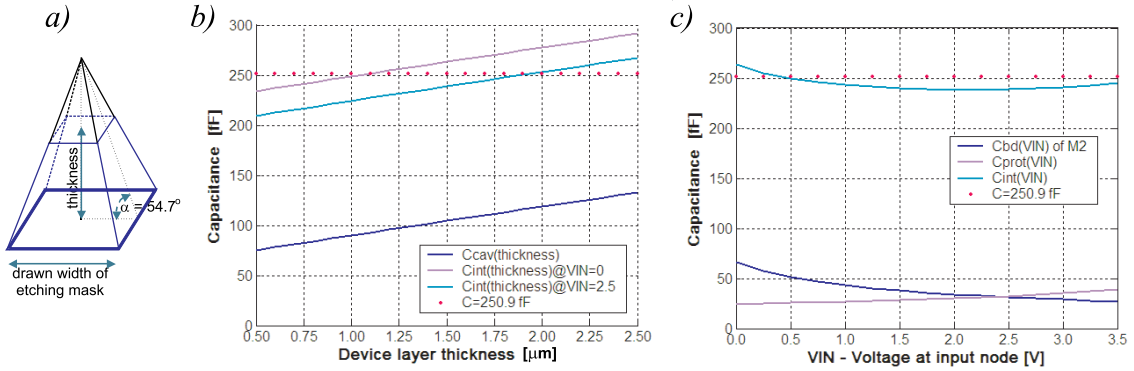


Figure 6.8: a) Pixel cavity geometry used for the calculations of the charge integrating capacitance - blue lines indicate the walls of the pixel cavity; b) C_{int} as a function of the device layer thickness and c) C_{int} as a function of the voltage level at the input of the readout channel.

value of C_{prot} increases when the voltage at the input node rises. For this reason, the changes of both capacitances partially compensate one another, as it is illustrated in figure 6.8-c. Assuming the nominal value of the integrating capacitance of:

$$C_{int} = 250.9 \text{ fF}$$

it translates into the maximum deviation of the integrating capacitance of 5.3 %.

The voltage-dependent character of the integrating capacitance together with the non-linearity of the readout channel results in the non-linearity of the charge-to-voltage gain. The theoretical shape of the characteristic of the charge-to-voltage gain versus the input voltage is presented in figure 6.9. For the approximate gain value of:

$$G_{Q \to V} = 3.51 \text{ mV/fC}$$

corresponding to:

$$G_{N_q \to V} = 0.57 \ \mu\text{V/e}^-$$

the maximum gain variation of 5.3 % is estimated for the input voltage ranging from 0 V to 3.5 V.

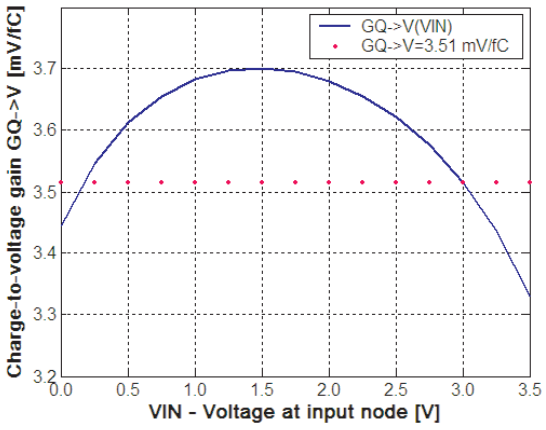


Figure 6.9: Estimated charge-to-voltage gain of the SOI detector test structures versus the input voltage.

6.1.3 Evaluation of Noise Performance

The charge-to-voltage gain calculated above determines the sensor sensitivity to the charge generated in its active substrate and collected on a detector electrode. Another important parameter of an active sensor is the signal-to-noise ratio (SNR) that sets the lower limit of the dynamic range of the device. In the case of pixel detectors with

charge division and analogue readout, the signal-to-noise ratio limits also the precision of the position measurement[1], which is given by [22]:

$$\Delta x \approx \frac{pitch}{SNR} \tag{6.12}$$

The noise performance of a monolithic active pixel sensor is determined by the noise associated with the readout electronics and the leakage current of the detector diodes. The main noise sources in the proposed monolithic active pixel sensors realized in SOI technology will be discussed in the following paragraphs.

Noise Sources in SOI sensors

The main noise sources in CMOS readout circuits operating at strong inversion are thermal noise and flicker noise, which is also known as 1/f noise. The thermal noise is related to the random motion of free carriers in the conducting resistive channel of a MOS transistor and is typically modelled as the white Gaussian noise with zero mean value. The current spectral density of the channel thermal noise depends on the operation region of the MOS device. In the case of the linear region, in which the inverse channel can be treated as a homogeneous resistance, it is given by [94]:

$$i_{n,t}^2 = 4kTg_{ds,lin} \tag{6.13}$$

where $g_{ds,lin}$ is the channel conductance in the linear region. In the saturation region, in which the transistor channel is classically modelled as a non-uniformly distributed transmission line, the noise current spectral density is obtained by summing the local thermal noise contributions to the total drain current fluctuations. For an ideal, long channel transistor, it is described by [95]:

$$i_{n,t}^2 = 4kTn\frac{2}{3}g_m \quad \text{for strong inversion} \tag{6.14}$$

$$i_{n,t}^2 = 4kTn\frac{1}{2}g_m \quad \text{for weak inversion} \tag{6.15}$$

where the n factor is given by equation 5.7.

Apart of the mentioned above thermal noise of a conductive channel, in the case of the readout electronics for the SOI sensor, the thermal noise associated with the bulk resistance may also play an important role due to the increased bulk sheet resistance

[1]Measurement precision of a position sensitive detector is defined as the root-mean-square distance of the measured coordinate from the true hit position.

in SOI technology. The contribution of this noise source depends on the transistor geometry and can be minimized by placing a bulk contact close to the transistor channel.

The flicker noise is the noise source that dominates at low frequencies. There are two main theories explaining the origin of the flicker noise: the number fluctuation model introduced by McWhorter [96] and the mobility fluctuation model described by the Hooge's equation [97]. First of the models attributes the flicker noise to the random trapping and detrapping of mobile carriers in the traps located at the $Si-SiO_2$ interface and within the gate oxide. The second model ascribes the flicker noise to the mobility fluctuations of the free carriers, which result from the carriers collisions with the crystal lattices. In SPICE level 2 and 3 models, the noise current spectral density of the flicker noise is expressed by:

$$i_{n,f}^2 = \frac{\mathrm{KF} I_D^{\mathrm{AF}}}{f^{\mathrm{EF}} C_{ox} L^2} \tag{6.16}$$

where I_D is the transistor drain current at operating point and KF, AF, EF are Spice model parameters, specific for particular CMOS technology. The measured values of these parameters for the technology of the SOI sensor are reported in [98].

The main noise source associated with the leakage current I_{leak} of a pixel diode is the shot noise that results from the random process of the charge carriers transition through a potential barrier. The shot noise is modelled as the white Gaussian noise with zero mean value and the noise current spectral density expressed by:

$$i_{n,s}^2 = 2qI_{leak} \tag{6.17}$$

Apart of the mentioned intrinsic noise sources, the output signal fluctuations in monolithic active pixel sensors can be also caused by electromagnetic interferences, power supply fluctuations and switching noise associated with digital signals. In the case of the SOI sensor test structures, these fluctuations are minimized by special layout design - leading digital signals by two parallel lines with opposite polarization and applying guardring structures around every sensor cell and the whole matrix.

Noise Analysis for SOI Sensor Test Structures

Precise analysis of the noise performance of the SOI sensor is a complicated task since it requires a non-stationary approach due to the switching operation of the readout circuit. Additional difficulty is introduced by the non-linearity of the charge-to-voltage conversion ratio. Example of an extensive noise analysis performed

for CMOS MAPS can be found in [99, 100, 101]. The reported approach, including a non-steady state readout circuit model and non-stationary noise sources, may be also applied with minor modifications for the monolithic active pixel sensor realized in SOI technology. Nevertheless, for the purpose of this work only simplified noise analysis will be presented in the following paragraphs. The evaluation of the noise performance will be performed separately for the particular phases of the readout circuit operation: the reset (i.e. discharging) of the integrating capacitance, the charge integration and the readout. The noise generated during the readout will be calculated directly at the output node, while the noise generated during the reset and the integration will be calculated as sampled on the integrating capacitance and transferred to the output during the readout phase.

Noise analysis for the reset phase

As mentioned, in the case of the readout circuit implemented on the SOI sensor test structures, the charge integrating capacitance is periodically discharged to remove collected charge and restore the baseline voltage at the input of the readout cell. However, there is always an uncertainty in the restored voltage level as the result of the channel thermal noise of the reset transistor. This uncertainty leads to so called reset noise (also known as kTC noise).

Both time domain and frequency domain approaches have been proposed in literature in order to calculate the noise generated during the reset phase [99, 100]. Since in the proposed SOI sensor test structures, the reset transistor always operates in the strong inversion during the discharging phase and the steady state is quickly achieved, the frequency domain method may be applied for the reset noise calculation. In such an approach, the simplified circuit representation illustrated in figure 6.10-a can be used for the reset phase. In this figure, the resistance R represents the channel resistance of the reset transistor (denoted by M2 in figure 6.5 and 6.2). Since the total integrated mean square noise of a system can be generally calculated as:

$$\overline{V_n^2} = \int_0^\infty v_n^2(f)|H(f)|^2 df \tag{6.18}$$

where $v_n(f)$ is the voltage noise spectral density of the noise source and $H(f)$ is the frequency response of the system, the following expression for the integrated mean square reset noise is easily obtained:

$$\overline{V_{n,res}^2} = \int_0^\infty 4kTR\frac{1}{1+(2\pi fRC_{int})^2}df = \frac{kT}{C_{int}} \tag{6.19}$$

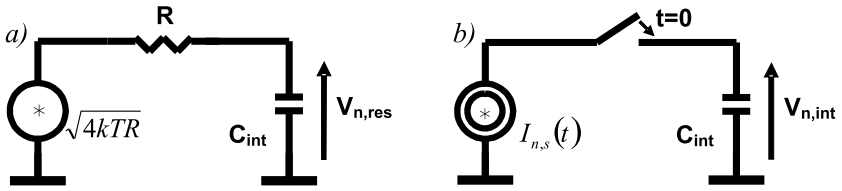


Figure 6.10: Simplified noise model of the SOI sensor a) at the reset phase and b) at the integration phase.

As mentioned, the reset noise expressed by the above equation is transferred to the output during the readout. Thus, for low and moderate frequencies, the output referred r.m.s. noise due to discharging of the integrating capacitance can be calculated by multiplying $\overline{V_{n,res}}$ by the low frequency gain of the source follower k_{u0}. However, it is usually more convenient to express the noise performance of a detecting system in terms of the equivalent noise charge (ENC)[2]. In general, this quantity is defined as the equivalent charge that corresponds to the output signal with the amplitude equal to the r.m.s. noise $\overline{V_{n,o}}$ at the output of the system and it illustrates the minimum input charge signal that may be distinguished by the detecting system. The ENC can be calculated as the ratio of the total integrated output r.m.s. noise and the output signal amplitude corresponding to one electron charge:

$$ENC = \frac{\overline{V_{n,o}}}{G_{N_q \to V}} \tag{6.20}$$

Taking into account equations 6.2, 6.3 and 6.19, one obtains the following expression for the equivalent noise charge associated with the reset phase ENC_{res}:

$$ENC_{res} = \frac{\sqrt{kTC_{int}}}{q} \tag{6.21}$$

The C_{int} capacitance in the above equation is approximately equal to the integration capacitance at zero input voltage.

[2]ENC is traditionally used for describing the noise performance of detecting systems. However, in the case of monolithic active pixel sensors it should be often referred to the expected charge signals since the number of the charge carriers generated by MIP particles may differ by an order of magnitude in different types of the monolithic sensors.

Noise analysis for the charge integration phase

During the integration time, i.e. when the reset transistor M2 is off and the charge generated in the sensitive substrate along with leakage current is integrated on the capacitance C_{int}, the main noise source in the monolithic active pixel sensor is the shot noise associated with the leakage current of a pixel diode. In order to calculate the total integrated mean square noise voltage $\overline{V_{n,int}^2}$ sampled on the integrating capacitance at the end of the integration time, the integrator structure presented in figure 6.10-b may be considered. The source $I_{n,s}(t)$ in this figure represents a shot noise current generator with the spectral density described by equation 6.17. Assuming that the switch is closed for the integration time of t_{int} and neglecting the changes of the integrating capacitance during the integration time, the mean square noise generated during the integration phase may be calculated as:

$$\overline{V_{n,int}^2} = \frac{1}{C_{int}^2} \int_0^{t_{int}} \int_0^{t_{int}} \overline{I_{n,s}(t_1) I_{n,s}(t_2)}\, dt_1 dt_2$$

Since the noise associated with the leakage current is white noise with the autocorrelation function of $\frac{i_{s,n}^2}{2}\delta(t)$, the following expression is consecutively obtained:

$$\overline{V_{n,int}^2} = \frac{qI_{leak}}{C_{int}^2} \int_0^{t_{int}} \int_0^{t_{int}} \delta(t_1 - t_2) dt_1 dt_2 = \frac{qI_{leak}}{C_{int}^2} t_{int} \tag{6.22}$$

The corresponding equivalent noise charge due to the integration phase is described by:

$$ENC_{int} = \sqrt{\frac{I_{leak} t_{int}}{q}} \tag{6.23}$$

Noise analysis for the readout phase

When a particular cell of the sensor matrix is selected and the readout phase begins, the main noise sources in the SOI sensors are the thermal and flicker noises of the follower transistor M1, the current source M4 and the row and column selection transistors Mrow and Mcol. The noise analysis of the SOI sensor test structures may be performed separately for the thermal noise and flicker noise sources.

Under assumption of the circuit steady state, a conventional frequency domain noise analysis may be efficiently performed for the thermal noise [54, 99, 100]. The circuit model useful for the noise calculation is presented in figure 6.11. For simplicity, the conductances g_{dscol} and g_{dsrow} in this figure represent:

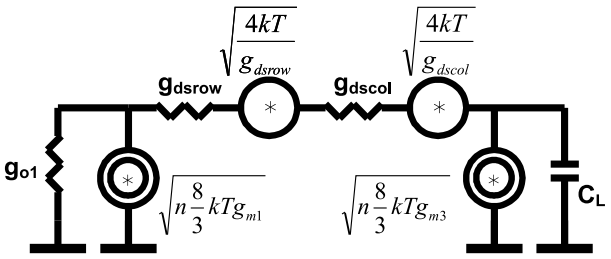


Figure 6.11: Simplified noise model of the SOI sensor at the readout phase.

- The sum of the output conductances of the NMOS and PMOS transistors building the column and row selection transmission gates for the readout cell configuration presented in figure 6.2-b
- The output conductance of the NMOS switch transistor for the cell configuration presented in figure 6.2-a

Other elements of the model - C_L and g_{o1} - denote the total load capacitance at the output of the readout circuit (approximately 1.2 pF) and the equivalent conductance seen from the source of the transistor M1, respectively. Due to the capacitive character of the signal source in a semiconductor detector, the conductance g_{o1} is expressed by:

$$g_{o1} = \frac{g_{m1}}{1+m} \tag{6.24}$$

where $m = C_{gs1}/C_{int}$.

Relying on the presented noise model, one obtains the following output referred mean square noise voltages due to the M1, Mrow, Mcol and M3 transistors, respectively:

$$\begin{aligned}\overline{V^2_{n,t,M1}} &= \int_0^\infty 4kTn\frac{2}{3}\frac{(1+m)^2}{g_{m1}}\frac{1}{1+\left[2\pi fC_L\left(\frac{1}{g_{o1}}+\frac{1}{g_{dsrow}}+\frac{1}{g_{dscol}}\right)\right]^2}df \\ &= n\frac{2}{3}\frac{kT}{C_L}\frac{(1+m)^2}{1+m+g_{m1}(r_{dsrow}+r_{dscol})}\end{aligned} \tag{6.25}$$

$$\begin{aligned}\overline{V^2_{n,t,Mrow}} &= \int_0^\infty 4kT\frac{1}{g_{dsrow}}\frac{1}{1+\left[2\pi fC_L\left(\frac{1}{g_{o1}}+\frac{1}{g_{dsrow}}+\frac{1}{g_{dscol}}\right)\right]^2}df \\ &= \frac{kT}{C_L}\frac{g_{m1}r_{dsrow}}{1+m+g_{m1}(r_{dsrow}+r_{dscol})}\end{aligned} \tag{6.26}$$

$$\overline{V^2_{n,t,Mcol}} = \int_0^\infty 4kT \frac{1}{g_{dscol}} \frac{1}{1 + \left[2\pi f C_L \left(\frac{1}{g_{o1}} + \frac{1}{g_{dsrow}} + \frac{1}{g_{dscol}}\right)\right]^2} df$$

$$= \frac{kT}{C_L} \frac{g_{m1} r_{dscol}}{1 + m + g_{m1}(r_{dsrow} + r_{dscol})} \tag{6.27}$$

$$\overline{V^2_{n,t,M3}} = \int_0^\infty 4kTn\frac{2}{3} g_{m3} \left(\frac{1}{g_{o1}} + \frac{1}{g_{dsrow}} + \frac{1}{g_{dscol}}\right)^2 \frac{1}{1 + \left[2\pi f C_L \left(\frac{1}{g_{o1}} + \frac{1}{g_{dsrow}} + \frac{1}{g_{dscol}}\right)\right]^2} df$$

$$= n\frac{2}{3}\frac{kT}{C_L}\frac{g_{m3}}{g_{m1}}[1 + m + g_{m1}(r_{dsrow} + r_{dscol})] \tag{6.28}$$

The total output referred mean square noise voltage associated with the thermal noise and generated during the readout may be consecutively calculated as:

$$\overline{V^2_{n,t,read}} = \overline{V^2_{n,t,M1}} + \overline{V^2_{n,t,Mrow}} + \overline{V^2_{n,t,Mcol}} + \overline{V^2_{n,t,M3}} = \frac{kT}{C_L} f(g_{m1}, g_{m3}, r_{dsrow}, r_{dscol}) \tag{6.29}$$

where $f(g_{m1}, g_{m3}, r_{dsrow}, r_{dscol})$ is a factor depending on the readout circuit operating point and the transistors dimensions. Taking into account above equation along with the equations 6.3 and 6.20, the formula describing the ENC due to the thermal noise of resistive channels of transistors is given by:

$$ENC_{t,read} = \frac{\sqrt{kT}}{qk_{u0}} \frac{C_{int}}{\sqrt{C_L}} \sqrt{f(g_{m1}, g_{m3}, r_{dsrow}, r_{dscol})} \tag{6.30}$$

Computing the output referred mean square noise voltage due to the flicker noise is not straightforward. It has been demonstrated in literature [99, 101] that precise noise analysis of switched circuits requires a non-stationary flicker noise model. Nevertheless, since the flicker noise is expected to be of a minor importance in the SOI sensor, only a standard frequency domain analysis, performed by means of conventional flicker noise models, will be described. In addition, it will be limited only to the contribution of the input transistor M1.

In order to calculate the flicker noise contribution into the equivalent noise charge of the SOI sensor, the readout circuit model similar to the one presented in figure 6.11 may be used. This time, however, the noise sources should be replaced by flicker noise generators characterized by the power spectral density expressed by equation 6.16. Using such a modified noise model of the readout circuit, the following integral describing the total output referred mean square noise voltage associated with the flicker noise and generated during the readout is obtained:

$$\overline{V^2_{n,f,M1}} = \int_0^\infty \frac{\mathrm{KF} I_D^{\mathrm{AF}}}{f^{\mathrm{EF}} C_{ox} L^2_{M1} g^2_{o1}} \frac{1}{1 + \left[2\pi f C_L \left(\frac{1}{g_{o1}} + \frac{1}{g_{dsrow}} + \frac{1}{g_{dscol}}\right)\right]^2} df \tag{6.31}$$

where L_{M1} is the channel length of the transistor M1. Analytical solution of the above equation has a complicated form. A numerical solution leads to the r.m.s noise voltage due to the flicker noise and the readout of order of 10 μV for the input transistor transconductance of 95 μS. This value translates into the equivalent noise charge of over a dozen electrons. As it will be demonstrated in next paragraphs, the obtained value of the ENC due to the flicker noise is negligible in comparison with other noise contributions.

Total noise optimisation of SOI sensor test structures

Total equivalent noise charge due to the reset, integration and readout phases can be calculated as:

$$ENC_{tot} \approx \sqrt{ENC^2_{res} + ENC^2_{int} + ENC^2_{t,read}} \tag{6.32}$$

According to formula 6.21, for a given temperature, the first contribution to the ENC_{tot} dependents only on the value of the integrating capacitance at zero input voltage $C_{int}(V_{IN} = 0)$. However, as presented in table 6.1, this value is determined to a large extend by the construction of the pixel cavity and the junction capacitance associated with the drain diffusion of the reset transistor M2. Since the drain area of this transistor has the minimum dimensions available in the CMOS technology provided by IET, minimizing integrating capacitance cannot be performed without significant modifications of the processing technology. In addition, the value of the integrating capacitance has to be adjusted to the requirements of the wide dynamic range of the sensor. For this reason, the equivalent noise charge of the SOI sensor test structures for the reset phase cannot be improved by optimisation of the readout cell. For the computed earlier integrating capacitance of $C_{int}(V_{IN} = 0) \approx 263.3$ fF and the temperature of 23 °C, ENC_{res} equals $ENC_{res} = 205$ e$^-$.

The given above value of the equivalent noise charge due to the reset phase contributes significantly to the total noise charge. In order to remove the reset noise (i.e. kTC noise) from the total noise of active sensors, the signal processing called correlated double sampling has been proposed in literature [102]. The principle of the CDS processing will be discussed later.

As given by formula 6.23, the contribution to the total equivalent noise charge due to the integration phase strongly depends on the leakage current of the pixel diode and the integration time. First of those parameters is determined by the quality of the sensor technology. As it was discussed in previous chapter, the leakage currents ranging from several to several hundreds of nanoamps per square centimeter were measured for the best diodes manufactured in the developed technology. These typically high and non-uniform leakage currents may lead to relatively high and varying from one sensor to another noise generated during the integration phase. In order to minimize the noise, short integration time should be set. The value of the ENC_{int} as a function of the integration time t_{int} and the leakage current normalized to the area of one square centimeter is presented in figure 6.12. As illustrated, for the integration time of 100 μs, acceptable noise level of 200 r.m.s electrons may be obtained even for the leakage currents of 400 nA/cm^2. Nevertheless, the integration time is often related to the minimum time required for the readout of the whole sensor matrix. In the case of the SOI sensor test structures, it typically equals 420 μs. Assuming the sensor leakage current of 200 nA/cm^2, it translates into the equivalent noise charge due to the integration phase of $ENC_{int} = 299$ e$^-$.

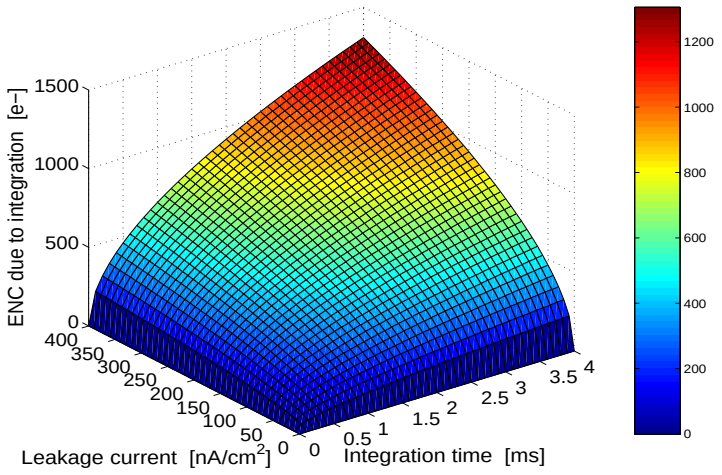


Figure 6.12: Equivalent noise charge of the SOI sensors due to the integration phase as a function of the integration time and the normalized leakage current.

This significant contribution dominates the total inherent noise of the SOI sensor. Reduction of this contribution would require making the integration time independent on the readout time. However, in such a solution, sensor dead time would arise during the time period between the end of integration time and the beginning of the readout time, which is unacceptable in many applications.

Last important input to the total equivalent noise charge is $ENC_{t,read}$. As described by equation 6.30, it is a function of the load capacitance C_L and the dimensionless factor f related to the operating point of the readout circuit. The values of the latter parameter as a function of the selection switches resistances and the input transistor transconductance are presented in figure 6.13. The results are computed assuming $r_{dsrow} = r_{dscol}$, constant value of the current source transconductance g_{m3} and constant value of the bias current. As illustrated, increasing the resistance of the selection switches limits the circuit bandwidth, and thus, reduces the resultant contribution of M1, Mrow and Mcol transistors to the f factor. Nevertheless, for higher r_{dsrow} and r_{dscol} resistances, the contribution of the current source transistor may become important. For this reason, in order to improve the noise performance of the SOI sensor during the readout phase, the cell selection switches should be characterized by low series resistance for a wide range of the input signals and the transconductance ratio of the current source and the follower transistor should have a small value. In the SOI sensors test structures, it is achieved by the usage of the selection switches in the form of transmission gates and by the design of the current source transistor with the width-to-length ratio of 1. As the result, assuming the input transistor transconductance of 95 μS, the value of the f factor of approximately 1.8 is obtained for the readout circuit with the row selection switches in the form of transmission gates

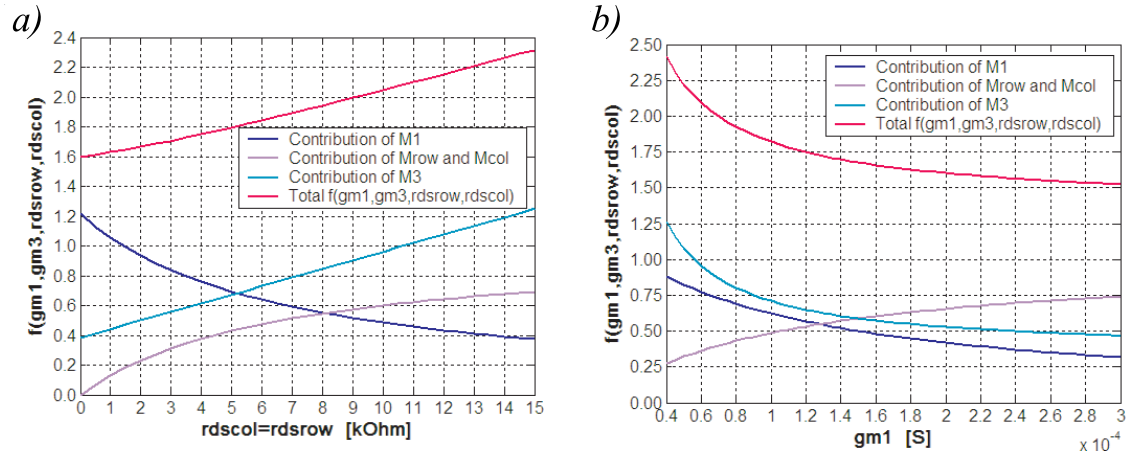


Figure 6.13: $f(g_{m1}, g_{m3}, r_{dsrow}, r_{dscol})$ factor determining the thermal noise due to the readout phase as a function of: a) the resistance of the channel selection switches ($g_{m1} = 95\ \mu S$) and b) the transconductance of the follower transistor ($r_{dsrow} = r_{dscol} = 6\ kOhms$).

(figure 6.2-b) and only slightly higher value of the f factor (up to 2.3) is achieved for the readout circuit with the single-transistor row selection switch (figure 6.2-a).

Figure 6.13-b shows that increasing value of the input transistor transconductance g_{m1} has a beneficial effect on the SOI sensor noise performance. It is worth to point out, that higher value of g_{m1} allows also using larger load capacitance C_L without reduction of the circuit bandwidth, which translates into further reduction of the equivalent noise charge of the SOI sensor during the readout phase. The advisable high values of the transconductance may be achieved by either increase of the bias current or the transistor width. However, in the first case, the transconductance of the current source M3 becomes higher, too; consequently, the resultant total value of the f factor may be enlarged. For this reason, the increase of the input transistor transconductance should be realized by designing the input transistor with a high width-to-length ratio. Since larger dimensions of the input device result also in larger integrating capacitance, there is an optimum value of the follower transistor width and transconductance. Assuming the bias current of 20 μA, the value of the equivalent noise charge of the SOI sensor test structures as a function of the input transistor transconductance is presented in figure 6.14. This figure illustrates the effect of the increasing follower transistor dimensions on the equivalent noise charge due to both reset and readout phases. As presented, the minimum value of the ENC due to the readout phase is achieved for g_{m1} of 135 μS, but taking into account additionally the ENC due to the reset phase, the optimum value of the g_{m1} shifts to 100 μS. The obtained optimal values of the transconductance translate into the dimensions of the input transistor of $W/L = 48\mu\text{m}/3\mu\text{m}$ or $W/L = 45\mu\text{m}/3\mu\text{m}$, respectively. In view of the limited area of a single cell of a pixel detector, the width of the input device of the designed test structure was reduced to 40 μm, which corresponded to the transconductance of 95 μS. This value is high enough to prevent from significant degradation of the noise performance for CDS processed or single sampled signals.

Summing up the particular noise contributions due to the reset, integration and readout phases leads to the total equivalent noise charge ENC_{tot} of the SOI sensor test structures of approximately 391 e^- for the leakage currents of 200 nA/cm^2, the integration time of 420 μs and room temperature. Nevertheless, as presented in figure 6.12, the equivalent noise charge may significantly increase for higher leakage current values, which emphasizes the importance of the quality improvement of the detector junctions in the further SOI sensor development.

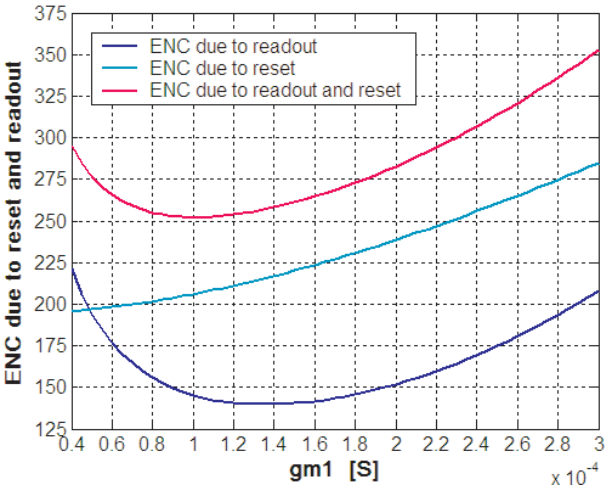


Figure 6.14: Equivalent noise charge of the SOI sensors due to the readout and reset phases as a function of the follower transistor transconductance. Results presented assuming constant bias current of 20 μA, $r_{dsrow} = r_{dscol} = 6$ $kOhms$ and temperature of 296 K.

Noise performance of the SOI sensor test structures after CDS processing

As mentioned, correlated double sampling (CDS) processing is a technique commonly used for the suppression of the reset noise of active pixel sensors. This technique takes advantage of the significant difference of the frequency bandwidth of the circuit presented in figure 6.10-a for the reset and integration phases. Since for the "off" state of the reset transistor, the bandwidth of this circuit is of order of several Hertz, the voltage uncertainty at the input node sampled at the end of the reset phase is hold throughout the integration phase. For this reason, the reset (kTC) noise may be removed by the subtraction of two consecutive signal samples taken after the reset.

The principle and the block diagram of the CDS processing is depicted in figure 6.15. As illustrated, the squared magnitude of the transfer function of the CDS processor is given by:

$$|H_{CDS}(f)|^2 = \left|1 - e^{-j2\pi f\tau}\right| = 4\sin^2(\pi f\tau) \tag{6.33}$$

where τ is the time delay between the two correlated samples. In practice, the readout chain preceding the CDS processor or the analogue-to-digital converter (ADC) is a low-pass filter with the cut-off frequency of f_{3dB} and the characteristic modelled by:

$$|H_{LP}(f)|^2 = \frac{1}{1 + \left(\frac{f}{f_{3dB}}\right)^2} \tag{6.34}$$

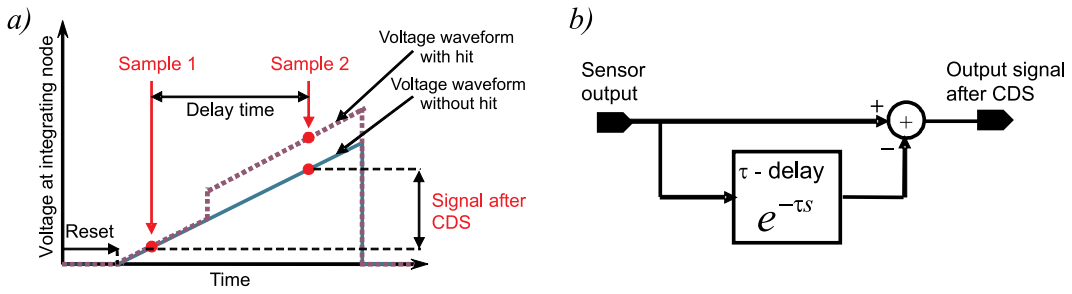


Figure 6.15: a) Principle of CDS processing; b) external CDS processor.

Therefore, the total processing path of the readout chain and the CDS processor has a band-pass characteristic described by:

$$|H_{LP,CDS}(f)|^2 = \frac{4\sin^2(\pi f\tau)}{1+\left(\frac{f}{f_{3dB}}\right)^2} \tag{6.35}$$

Due to the band-pass character, the CDS processor allows suppressing not only the reset noise, but also the low frequency noise components. However, comparing the transfer characteristics of the low-pass readout chain and the CDS processor, one observes that the CDS processing increases the contribution of the white noise. As the ratio of the white noise contribution after and before CDS processing equals to:

$$\frac{\int_0^\infty |H_{LP,CDS}(f)|^2 df}{\int_0^\infty |H_{LP}(f)|^2 df} = 2 \qquad \text{for} \quad f_{3dB}\tau > 1 \tag{6.36}$$

the CDS processing must be carefully used if the contributions of the white and kTC noises to the total noise of the SOI sensor are comparable.

6.1.4 Measurements of SOI Sensor Test Structures

The performance and the parameters of the SOI detector test structures were verified experimentally. Such important characteristics of a particle detector as the full depletion voltage, the charge-to-voltage conversion gain, the noise, the dynamic range and the leakage current were investigated. In particular, the results of the gain and noise evaluation were compared with the measurement results. This allowed examination of the accuracy of the parameters extraction and verification of the sensor design.

The details of the test procedures are described below. All the results presented in this section were obtained for the SOI sensor structures coming from the same wafer with the identification number of PT239. Other sensors, manufactured on the wafer PT234 and delivered for measurements, were not suitable for tests due to processing faults at the silicon foundry.

Observation of Output Signals from SOI Sensors

First step of the tests was the observation of the sensor response to the charge generated in the detector active volume by beta particles transmitted by Strontium-90 (Sr-90) radioactive source. For this purpose, the structures were packaged and assembled on universal printed circuit boards. Particular channels of the sensor were selected by microswitches and corresponding reset lines were steered by a voltage pulse generator. Since no readout digital control blocks were implemented on the test structures, the matrices with the readout cells presented in figure 6.2-a were chosen for these measurements to reduce the number of necessary external control signals. One of the sensor responses recorded by a digital oscilloscope is presented in figure 6.16. The waveform corresponds to two events, which occurred during the integration time of 2 ms in the detector volume underneath the selected channel. Along with the collection of the charge generated by ionising particle, the integration of the leakage current can be observed.

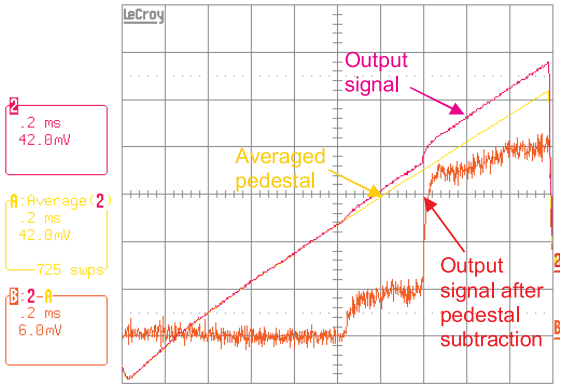


Figure 6.16: Multiple-event recorded in the SOI sensor test structure and observed by a digital oscilloscope (LeCroy 374). Orange line – the waveform observed at the output of the selected channel before the exposition of the sensor to the beta radiation; purple line – after placing the Strontium 90 source over the sensor; red line – the difference of the purple and orange waveforms.

Determination of Full Depletion Voltage

Since in many applications of semiconductor detectors (e.g. detection of short range particles or MIPs), it is important to operate the sensor at full depletion, one of the first parameters that were measured for the small-area SOI detectors was the voltage required for the formation of the space charge region in the total detector substrate. Although this parameter was measured earlier for other wafers, it had to be also found for the wafer PT239 due to possible variations of the resistivity of the sensor substrates.

The full depletion voltage could not be determined from the C-V characteristics of test junctions because the investigated wafer was not available for measurements before dicing. For this reason, an indirect measurement method was proposed. It based on the phenomena that the junction capacitance and the leakage current of a detector diode do not change significantly with increasing reverse bias voltage once the full depletion voltage is reached. Since, without exposure to radiation, the output signal of the SOI sensor depends only on the values of these two parameters, the full depletion voltage could be determined from the change of the output voltage measured for different detector bias voltage.

The measurements aiming at the determination of the full depletion voltage of the SOI sensor test structures were performed for four different chips. Two outermost rows and columns of the matrices were ignored in the analysis due to edge effects. The results obtained at the room temperature and the integration time of 500 μs are presented in figure 6.17. As illustrated, the value of the output voltage corresponding

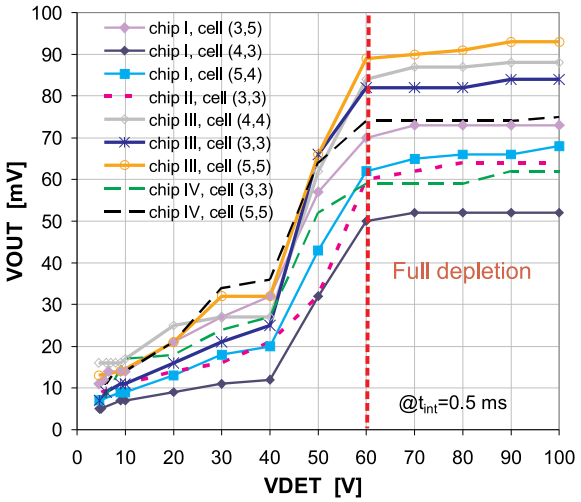


Figure 6.17: Results of the full depletion voltage measurements - sensor output voltage due to the integration of the leakage current as a function of the reverse bias voltage.

to the pixel leakage current integrated on the input capacitance becomes practically constant for the detector bias V_{DET} higher than approximately 60 V. This value was treated as the full depletion voltage in further tests of the SOI sensors produced on the wafer PT239.

Measurements of Charge-to-Voltage Conversion Gain

Another important characteristic that was examined for the proposed test structure of the SOI sensor was the charge-to-voltage conversion gain. A standard method of the conversion gain calibration in silicon detectors is the exploitation of the interaction of low energy gamma radiation with the detector material. As mentioned in chapter 2, the dominant absorption process for the photon energies up to several dozen keV is the photoelectric effect in which a photoelectron is produced. This photoelectron has energy approximately equal to the energy of the impinging photon and leads to the formation of electron-hole pairs. The number of the created electron-hole pairs equals to the ratio of the photon energy and the energy required for creation of one electron-hole pair in silicon. As the photon absorption by the photoelectric effect may be additionally treated as a point-like interaction, it especially suitable for the gain calibration of pixel sensors.

For the gain calibration of the SOI detectors, Americium-241 (Am-241) source was used. The gamma emission spectrum of this source distinguishes by gamma-peaks at the energies of 26.34 keV (with intensity of 2.4 %) and 59.54 keV (with intensity of 35.9 %) and an X-ray line at the energy of 13.9 keV (with intensity of 37 %) [103]. Since the absorption efficiency of the 60 keV photons in 400 μm silicon is of order of 5 % [104], a closed radioactive source with relatively high activity of 10 MBq was chosen for the measurements.

Test set-up

The calibration of the charge-to-voltage conversion gain was performed with the usage of the multifunctional data acquisition (DAQ) called SUCIMA Imager. The system was developed at the Institute of Nuclear Physics in Krakow for the purpose of the SUCIMA project [105]. A block diagram of the SUCIMA Imager is presented in figure 6.18. As illustrated, the system consists of four independent analogue input channels (each with 12 bit analogue-to-digital converters and 1MB fast Static RAMs), FPGA Virtex II XC2V1000 chip and high speed USB 2.0 port for data exchange with

a PC computer. During the tests of the SOI detector test structures, the SUCIMA board allowed the supervision of the functionalities required for analogue data readout, sampling, digitalisation, signal processing, data selection, storage and fast data transmission to a PC computer. In particular, it was used for the generation of the cell-selection signals for the sensor.

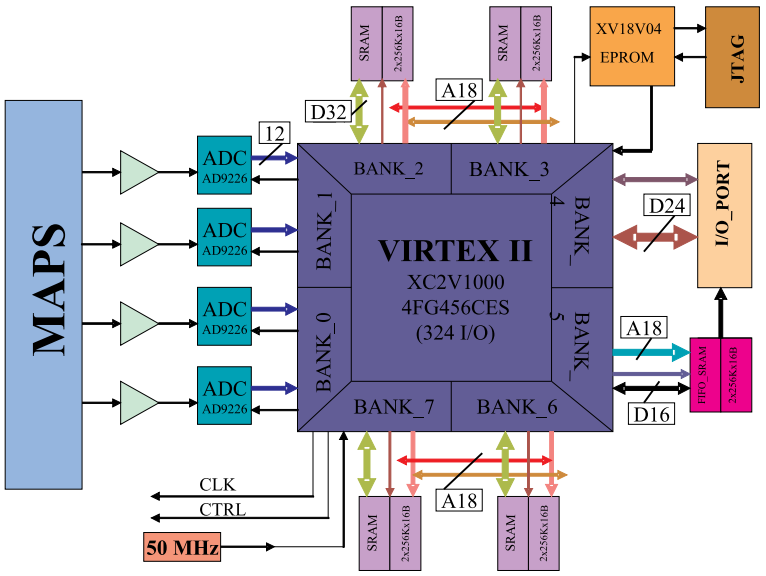


Figure 6.18: Architecture of the SUCIMA Imager board [105].

The readout sequence implemented in the Virtex FPGA is illustrated in figure 6.19. As presented, at the beginning of the control sequence, the whole sensor matrix was reset in a column-by-column order. After the discharging (i.e. reset) phase, the particular row and column selection signals were activated and the matrix was read out in series. In order to perform the CDS processing, the whole sensor was read out twice. First sample was taken immediately after the reset phase, while the second one was taken after the integration time, which was equal to the time required for a single readout of the whole matrix. These samples corresponded to "sample 1" and "sample 2" in figure 6.15, respectively. The difference of these two samples was computed on-line by the DAQ system and the result of the CDS processing was sent to a PC computer and stored on a hard disk.

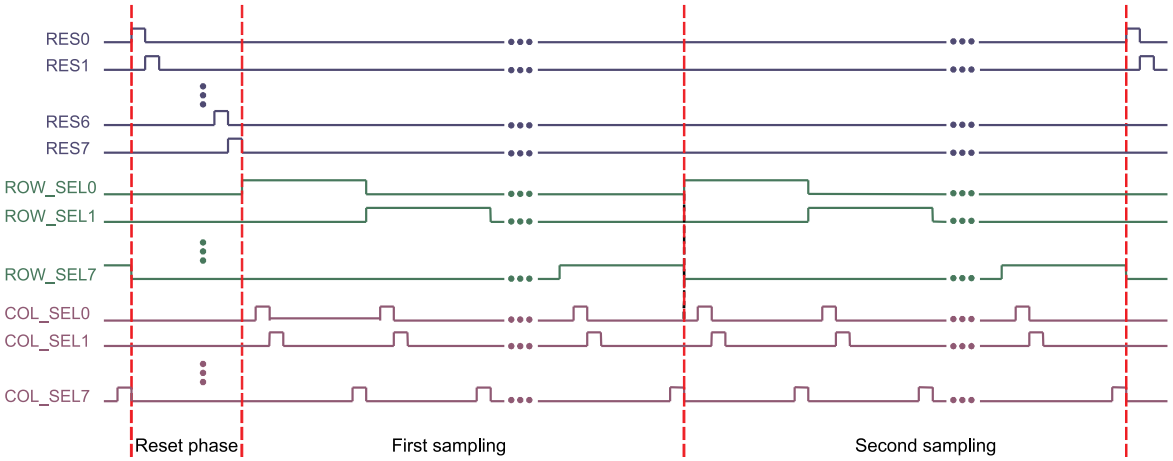


Figure 6.19: Readout sequence implemented on the SUCIMA Imager for the tests of the SOI detector test structures.

The DAQ system was connected to a graphical user interface (GUI) program developed in LabVIEW environment [83]. The interface enabled setting: the period of the readout clock, the ADC clock delay and the number of the readout runs. It also provided the CDS or "Last Frame" readout mode, masking noisy pixels, subtracting pedestals, suppressing signals bellow threshold and writing data to an ASCII file. Additionally, it allowed selection of the matrix size to be read out. This option was used to reduce the readout time at low clock frequencies. Since the detector test structures were not surrounded by pixel guardrings, usually the inner part of the chip, consisting of 6 by 6 channels, was read out. It corresponded to the integration time of 420 μs at the typical clock period of 10 μs.

The packaged detector structures were connected to the SUCIMA Imager via an adopting board in order to amplify the measured signals and adjust the voltage levels. The analogue processing path realized on the adopting board is illustrated in figure 6.20. First stage of the circuit is a buffer, which prevents overloading the sensor output. Next stage is made up of an operational amplifier with a negative feedback loop, which allows signal amplification by the factors of 1, 2, 4.7 or 10. The amplifier provides also the adjustment of the output voltage offset to the level appropriate for the last processing stage that converts the single ended signal to the deferential one. A photograph of the complete set-up used in measurements of the SOI test detectors is presented in figure 6.21.

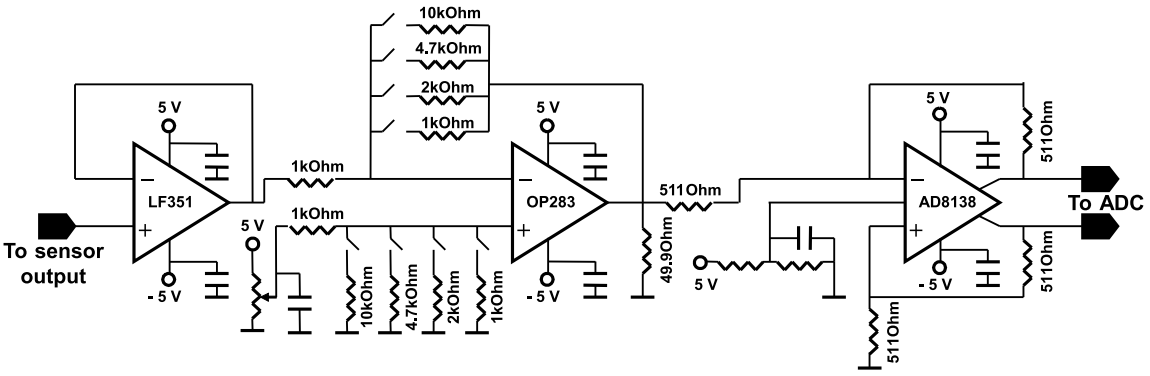


Figure 6.20: Analogue processing path realized on the adoption board for the tests of the SOI test sensors.

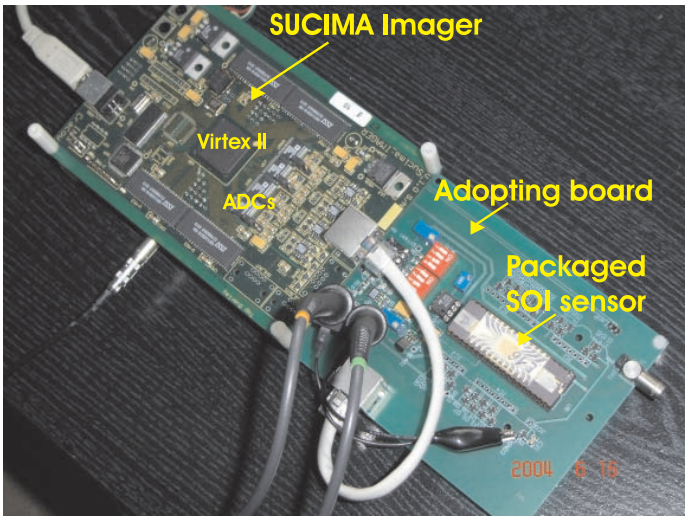


Figure 6.21: Photograph of the set-up used in the measurements of SOI test detectors.

Data analysis and results of conversion gain calibration

The calibration of the charge-to-voltage conversion gain was performed at room temperature and at the detector bias of 60 V. The integration time of 420 μs and the test set-up gain of 4.5 ADC counts per 1 mV were adjusted. To eliminate the reset noise, the CDS processing was performed on-line by the DAQ system. The collected data (845 thousands frames) were analysed off-line using MATLAB high-level language [106]. The algorithm used for the data analysis is illustrated in figure 6.22.

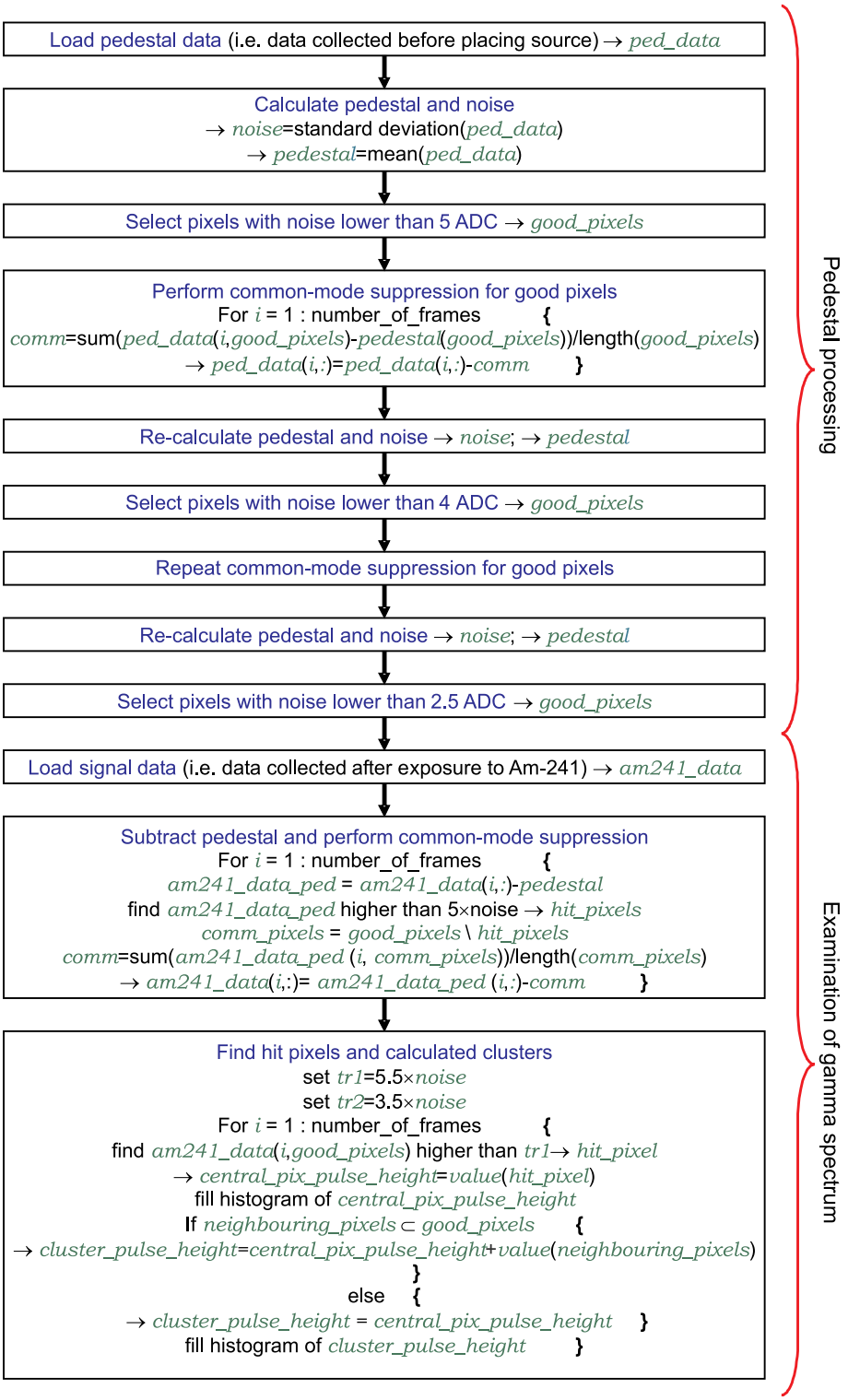


Figure 6.22: Algorithm of the data analysis performed for the calibration of the charge-to-voltage conversion gain with Am-241 source.

The data analysis was performed in two steps. First pedestal data, which had been collected before placing the radioactive source on the detector, were processed. The average pedestal value and the r.m.s noise were computed after two runs of the common-mode suppression algorithm[3]. To illustrate the effectiveness of the applied technique, the distributions of the measured pedestal data before and after the common mode suppression for one of the pixels are presented in figures 6.23-a and 6.23-b, respectively. As illustrated, the Gaussian shape of the pedestal distribution was restored and the standard deviation of the data was significantly reduced by

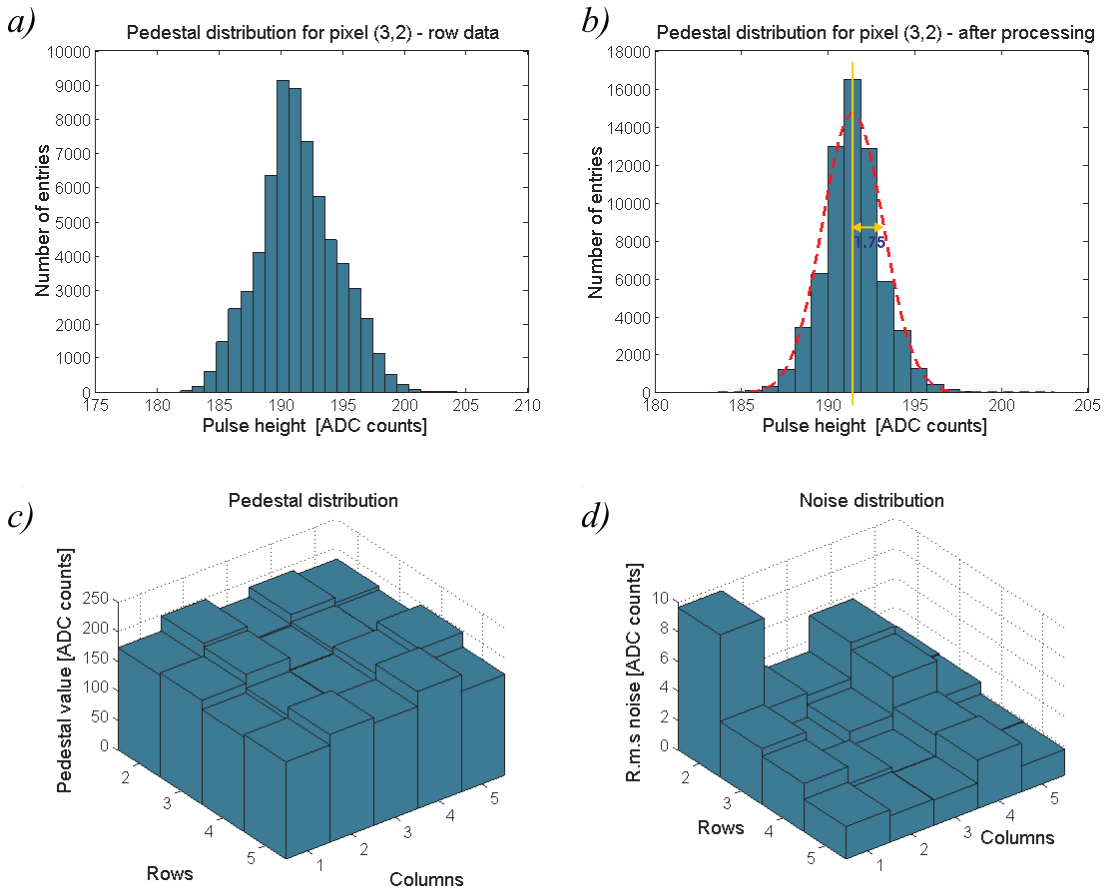


Figure 6.23: Pedestal distributions measured for the test structures of the SOI sensors: a) histogram of the pedestal values for a single pixel (row=3, column=2) obtained for row data, b) histogram of the pedestal values for a single pixel (3,2) obtained after the common-mode suppression, c) pedestal distribution over the sensor matrix and d) r.m.s. noise distribution over the sensor matrix after the common-mode suppression.

[3]Common-mode suppression allows elimination of the interferences that are common for the whole sensor matrix and typically result from fluctuations of supply voltage or electromagnetic interferences.

suppression of the common interferences. The calculated average pedestal signals and the values of the root mean square noise for every cell of the sensor are given in figures 6.23-c and 6.23-d. Like in previous paragraph, external rows and columns were not included in the analysis due to very high pedestal values and high noise. As given in figure 6.23-d, the r.m.s. noise below 2 ADC counts was measured for the best pixels.

Relying on the calculated r.m.s noise, good pixels of the sensor were selected for the examination of the gamma spectrum of the Americium-241 source. The pedestal value was subtracted from every data frame and the common-mode suppression was performed. During the common-mode suppression, the pixels on which the signal value higher than 6 times noise was found were skipped. Afterwards, the frames for which a photon was registered were extracted, the clusters were computed and the histograms were filled in.

Exemplary events registered by the SOI sensor are illustrated in figure 6.24-a. The graphs show typical cases when the 59.54 keV photons lead to the formation of a signal with the pulse high between 40 and 50 ADC counts on a single electrode of the sensor. Due to the chip operation in the charge integration mode, a frame with two events during the integration time was also found, which is illustrated on the second graph. Histogram of the signal pulse height obtained for one of the pixels is given in figure 6.24-b. Comparing this graph with the pedestal distribution of the same pixel (illustrated in figure 6.23-b), one distinguishes the histogram bars corresponding to the signal generated by gamma radiation. The scatter plot depicted in figure 6.24-c proves that the signals measured for different pixels are uncorrelated, and thus, can be treated as the result of the detection of the photons emitted by the radioactive source.

The complete gamma spectrum of the Am-241 source obtained after the cluster calculation and the corresponding histogram of the cluster size are finally given in plots 6.24-d and 6.24-e, respectively. As presented, the detection of a low energy gamma ray in the active substrate of the SOI sensor usually induces a signal on a single electrode of the device. However, wide spread of the measured signal values can be observed. In particular, the photo-peak related to the interaction of the 59.54 keV photon with the detector material is not well separated. This is partially due to the Compton scattering of the photons, which, as given in figure 2.3, plays quite important role in the investigated energy range. Additionally, overlapping of the peaks corresponding to the photon energies of 26.34 keV and 59.54 keV occurs because of the low charge-to-voltage conversion gain of the proposed configuration of the SOI sensor

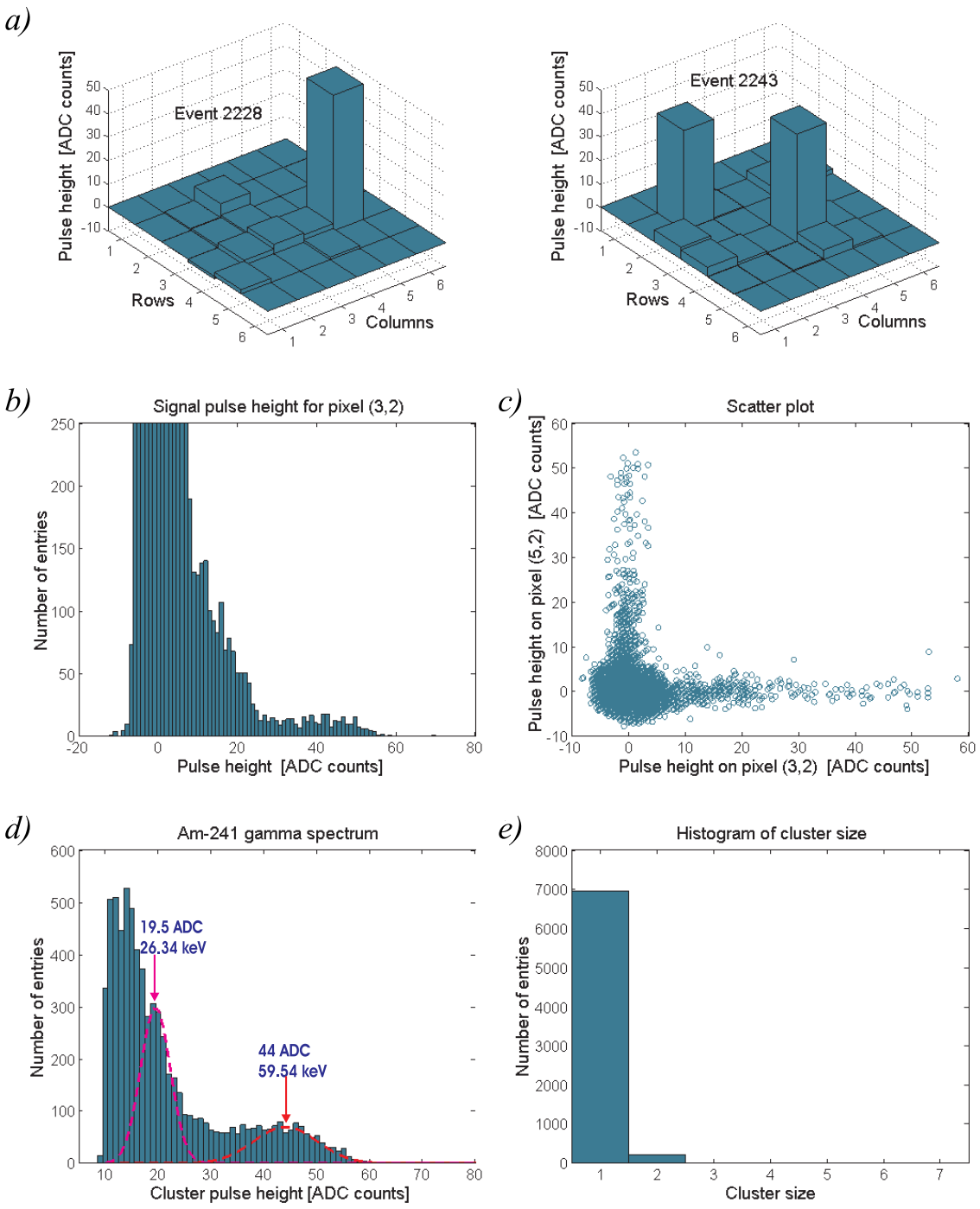


Figure 6.24: Results of the measurements of the Am-241 spectrum obtained with the test structures of the SOI detector: a) exemplary registered events, b) histogram of the signal pulse height measured for a single pixel (row=3, column=2), c) scatter plot illustrating the lack of the correlation between the signals measured for two different pixels, d) histogram of the cluster pulse height and e) histogram of the cluster size.

test structure. It should be underlined that in spite of the significant difference in the intensity of those two peaks, their heights on the spectrum registered with a silicon sensor do not diverge to a large extend as the result of the low absorption efficiency (about 5 %) of the photons with the energy of 59.54 keV in 400 μm thick silicon [104]. Significant width of the photo-peak at 59.54 keV - about 6 ADC counts with reference to the measured single pixel noise below 2 ADC counts - is also the effect of the pixel-to-pixel parameter variations and the operation of the sensor in an untriggered mode. The later is important only for the photons detected far from the pixel electrode and may result in partial collection of the charge coming from the same event within two subsequent frames. Last but not least, some spread of the measured signal results from the non-uniformity of the charge collection efficiency in the SOI sensors. As observed in simulations, the amount of the assembled charge depends on the position of the interaction point. According to the performed simulations, the variations of the collection efficiency do not exceed 5 %, which translates into the increase of the width of the photo-peak to about 3 ADC counts. In a real sensor, these variations may be more significant due to higher recombination velocity than assumed in the doping dependent model.

Despite significant width, the photo-peak corresponding to the detection of the gamma rays with the energy of 59.54 keV is found at 44 ADC counts. Taking into account the amplification of the test set-up and the energy required for the creation one electron-hole pair in silicon, the measured cluster pulse height translates into the following value of the charge-to-voltage conversion gain:

$$G_{Q\rightarrow V} = 3.71 \text{ mV/fC}$$

which corresponds to:

$$G_{N_q\rightarrow V} = 0.59 \ \mu\text{V/e}^-$$

The measured value of the charge-to-voltage conversion gain is in good agreement with the value estimated relying on the cell layout and the technological parameters provide by the manufacturer.

Taking advantage of the calibration of the charge-to-voltage conversion gain, the equivalent noise charge of the examined sensor could be calculated. The total ENC of approximately 670 e^- was obtained for the r.m.s. noise of order of 1.8 ADC counts measured for the complete system. To evaluate the noise performance of a bare SOI sensor, the set-up r.m.s. noise of 1 ADC count had to be included in the analysis.

Finally, the equivalent noise charge of order of:

$$ENC = 560 \text{ e}^-$$

was estimated for good pixels. Obtained result proves that no significant noise pick-up occurs in the designed test structures of the SOI sensors. In particular, the substrate coupling or the crosstalk between the readout electronics and the detector active substrate do not influence significantly the noise performance of the sensor. Nevertheless, the charge collection non-uniformities and the matching properties of the sensor cells result in the measured variations of measured signals.

Sensor Response to Minimum Ionising Electrons

Many particles produced in high energy experiments or present in cosmic-rays (e.g. cosmic-ray muons) are minimum ionising particles (MIPs). For this reason, the response of the proposed SOI sensor to this kind of particles was investigated. In particular, the most probably amount of the charge collected on a detecting electrode after the passage of a minimum ionising particle and the corresponding signal-to-noise ratio were measured.

The tests were performed with the use of the Strontium-90 (Sr-90) source. Strontium-90 is a radioactive isotope, which emits electrons as the result of two consecutive beta-decays:

$$^{90}_{38}Sr \rightarrow ^{90}_{39}Y + \beta^- \rightarrow ^{90}_{40}Zr + \beta^- \tag{6.37}$$

The probability of the electron emission for both decays is 100 %. The first transition is characterized by the half-life of 28.5 years and the maximum electron energy of 0.546 MeV, while the second transition – by the half-life of 64 hours and the maximum electron energy of 2.283 MeV [21]. The high energy beta particles produced in the Yttrium-90 decay deposit in silicon the energy similar to the minimum ionising particles, but the lower energy contributions cause a longer tail of the measured signal distribution.

The response to the beta particles emitted by the Sr-90 source was measured with the usage of the same set-up and sensor as in the previous point. The same settings of the data acquisition system and the adopting board were also applied. The detector was biased with 60 V and the integration time of 420 μs was adjusted. The Sr-90 source (with activity of 140 kBq) was not collimated during the measurements and

the DAQ system operated in an untriggered mode. Therefore, the beta particles might enter the sensor active volume at different angles and not all of the recorded electrons could be considered as MIPs. After the measurements, similar analysis like in the tests with the Americium-241 source was performed, but this time, it was limited to a small sub-matrix of 3 by 3 pixels and the $tr1$ threshold was set at 10 time noise of the central pixel of the cluster.

The results of the measurements and the subsequent analysis are presented in figure 6.25. First two plots show exemplary registered events. As presented, the amount of the energy deposited by the beta particle in the sensor sensitive substrate varies significantly. The complete histogram of the measured cluster pulse high is illustrated

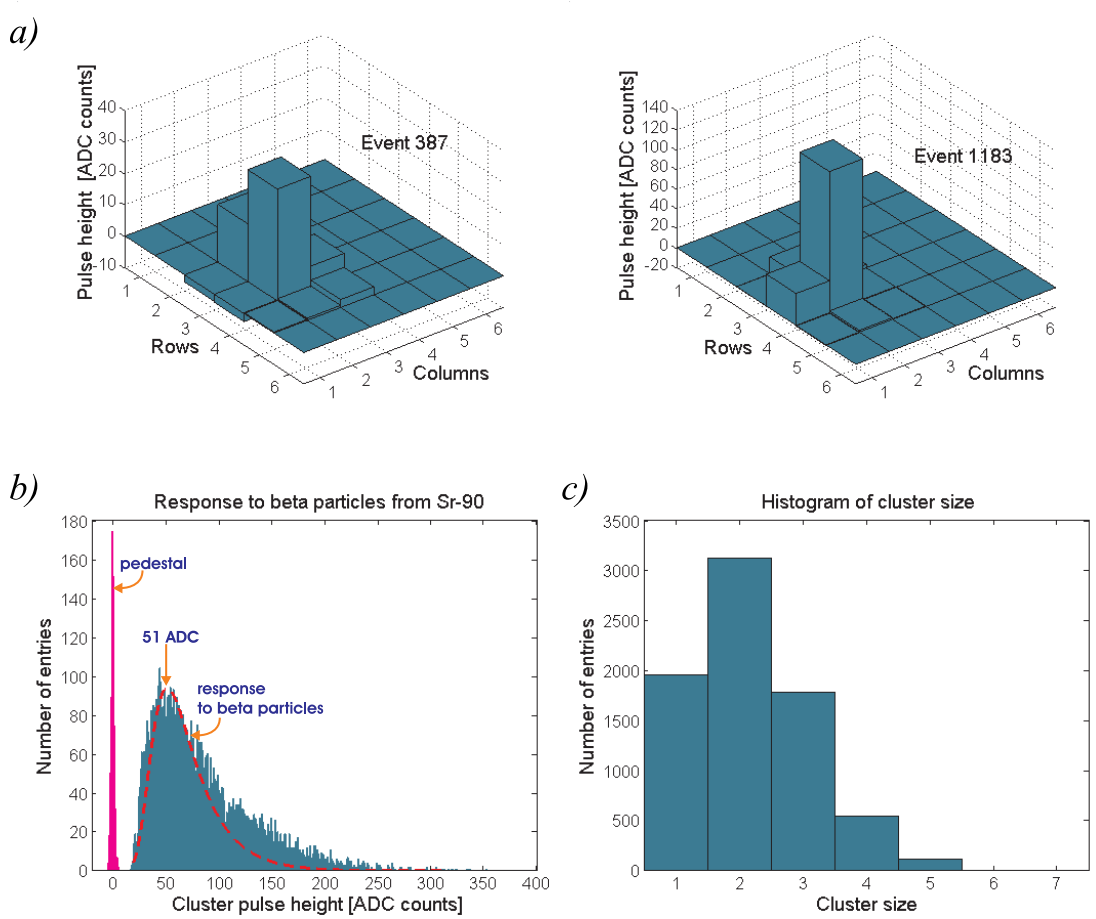


Figure 6.25: Measurements results of the sensor response to the beta particles from the Sr-90 source: a) exemplary registered events, b) histogram of the pedestal distribution after the subtraction of its average value (pink bars), histogram of the cluster pulse height measured after the exposition to the beta radiation from the Sr-90 source (turquoise bars) and the Landau fit (red line), c) histogram of the cluster size.

in figure 6.25-b. The sensor response to the electrons is juxtaposed with the pedestal distribution of the central pixel of the cluster. Basing on the numerical approximation given by 2.4, the histogram of the cluster pulse high was fitted to the Landau distribution and the signal value corresponding to the most probable energy deposition by a minimum ionising electron was extracted. The most probable cluster pulse height of 51 ADC counts was measured, which translated into the signal-to-noise ratio referred to the central pixel r.m.s noise of 30. As expected from simulations, the typical cluster size larger than 1 was also obtained.

Taking into account the calibrated charge-to-voltage conversion gain of the SOI sensor, the following value of the most probable charge collected on the sensor electrode after the passage of the beta particles emitted by the Sr-90 source was computed:

$$MIP\ charge = 19200\ \mathrm{e}^{-}$$

The obtained result is lower than expected. Relying on the thickness of the sensor substrate and the simulation results presented in figure 4.9-b the signal of approximately 29600 electrons was foreseen. In order to demonstrate that this result is not related to under-depletion of the sensor active substrate, the tests with the Sr-90 source were repeated for another chip at the detector bias of 70 V and at the set-up amplification of 2.5 mV per 1 ADC count. The most probably cluster pulse height of 27 ADC was obtained, which corresponded to the collected charge of 18300 electrons. Thus, the detector under-depletion was excluded as a possible reason of the charge loss.

The origin of the considerable charge loss is not understood completely, but it is expected that the recombination life time, just as the generation life time, in the active substrate of the manufactured SOI sensor is significantly lower than in good hybrid pixel detectors. However, this may be related to poor quality of the starting handle wafers. In order to prove this statement, comparison of the charge collection properties of the sensors produced on the wafers coming from different suppliers is required. Evaluation of the parameters the detector diodes manufactured on handle wafers and connected to external readout electronics would be also helpful. In order to accomplish such tests, a joint research effort with an SOI substrate manufacturer has been recently started.

Estimation of Leakage Current

Knowing the value of the charge-to-voltage conversion gain, the level of the leakage currents of the test matrices could be estimated. For this purpose, the sensor output voltage V_{OUT} after CDS processing for a particular charge integration time t_{int} was measured. The dark currents I_{leak} were computed for the pixels of sensor matrices taking into account the relation between the current and the collected charge Q_{coll}:

$$I_{leak} = \frac{dQ_{coll}}{t_{int}} \tag{6.38}$$

and the relation between the output voltage and the input charge, which is described by equation 6.1. The obtained results were subsequently normalized to the area of a square centimetre.

The leakage currents were estimated for 4 randomly selected test structures of the SOI sensors. For each tested chip, the characteristics of sixteen innermost pixels were examined. The results of the leakage current measurements obtained for the detector bias of 60 V and room temperature are summarized in table 6.2. The sensor identification numbers given in this table correspond to figure 6.17 for the chips I to IV. The structure labelled as "chip V" is the sensor used for the gain calibration. As presented, the typical normalized leakage currents of order of:

$$I_{leak} = 200 \text{ nA/cm}^2$$

were measured for the test structures of the SOI sensors produced on the wafer PT239. This value is in a good conformity to the results obtained during the wafer level measurements.

Table 6.2: Leakage currents evaluated for the test structures of the SOI sensors. Results obtained for the detector bias of 60 V and room temperature.

Sensor identification number	**Chip I**	**Chip III**	**Chip IV**	**Chip V**
Mean leakage current per pixel [pA/pixel]	34	45	36	26
Mean normalized leakage current [nA/cm^2]	201	266	212	151
Min normalized leakage current [nA/cm^2]	158	258	186	140
Max normalized leakage current [nA/cm^2]	224	281	234	166

Measurements of Linearity and Dynamic Range

Last parameter that was examined for the test structures of the SOI sensor was the linearity of the transfer characteristic. The first technique that was applied for the linearity assessment based on the measurements of the sensor response to an infrared laser pulse with adjustable width or to a different number of laser pulses with constant width. The tests were performed using unfocused laser light with the wavelength of 850 nm. The laser spot was shinned on the backplane of a fully depleted detector, biased by a metal mash with rectangular holes. The output of the selected pixel of the tested sensor was observed directly on the screen of a digital oscilloscope. 10000 waveforms were recorded for every pulse width or for every number of the laser pulses injected during the integration time and the results were averaged. The total number of the light pulses and the maximum pulse width were limited by the frequency response of the measurement set-up, the leakage current and some continuous light transmitted by the laser system. The cut-off frequency of the test set-up was of order of 100 kHz due to the direct connection of the sensor output with the input of the oscilloscope via a BNC cable.

Figure 6.26-a shows the sensor response to the laser light with various pulse width (form 0 to 118 μs), measured for the integration time of 500 μs and the detector bias voltage of 70 V. The value of the output voltage V_{OUT} is given after the CDS processing, but before the subtraction of the pedestal value. The obtained characteristic is juxtaposed with its linear fit. Relying on the results of the charge-to-voltage gain calibration, the input charge values corresponding to the output voltage at the endpoints of the characteristic are also marked. As illustrated, no limit of the dynamic range was observed in the investigated range and the maximum non-linearity of the sensor characteristic of 4.2 % was measured for the signals corresponding to the input charge from approximately 21 fC to 192 fC.

The sensor response to the different number of the laser pulses injected during the integration time of 1 ms is presented in figure 6.26-b. The displayed characteristic was measured for the detector bias of 60 V and the laser pulse width of 4 μs. Like in the previous point, the obtained results are juxtaposed with the linear fit of the transfer characteristic and the markers showing the amount of the collected charge. Again, no limit of the dynamic range was observed in the investigated range and the maximum non-linearity of 4.4 % was measured for the input charge from 33 fC to 171 fC. These results are in good agreement with the discussion performed in section 6.1.2.

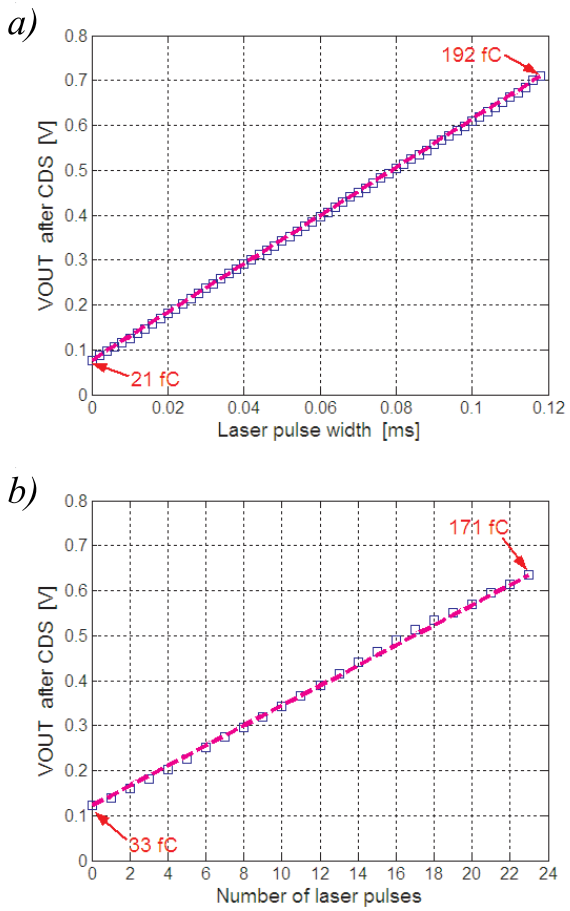


Figure 6.26: Linearity of the SOI sensor test structures measured with a laser spot: the sensor output voltage versus a) the laser pulse width (blue marker) and b) the number of laser pulses (blue marker). Pink dashed lines denote linear fits. Output voltage is given after CDS and without pedestal subtraction.

Since the described above method did not allow investigating of the full dynamic range of the sensor, complementary tests were performed for bare readout channels - with input pads instead of the sensing diodes. Both of the readout channel configurations presented in figure 6.2 were examined. The tests were performed for packaged readout matrices manufactured on low resistivity SOI wafers because they did not require presences of the pixel diodes. The matrices were assembled on dedicated printed circuit boards and the transfer characteristics of the readout channels were measured with a voltage pulse signal from the Agilent 33250A generator. The output signal observed on a digital oscilloscope versus the input voltage is presented in figure 6.27. Relying on the measured earlier charge-to-voltage conversion gain of 3.71 mV/fC, the approximate charge values corresponding to the endpoints of the obtained characteristics were also marked.

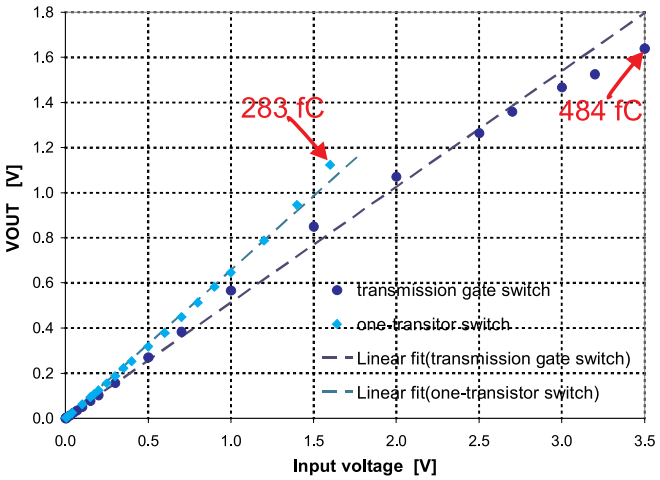


Figure 6.27: Results of the linearity measurements of the readout electronics for the SOI sensor - transfer characteristics of the readout channels with the row selection switches in the form of an NMOS transistor and a transmission gate.

As illustrated, the output dynamic ranges of 1.1 V and 1.6 V (and the corresponding input dynamic ranges of 283 fC and 484 fC) were obtained for the readout cells with the channel selection switches in the form of a NMOS transistor and a transmission gate, respectively. The first channel configuration was characterized by the non-linearity of 6.4 % in the investigated range, while the second one – by the non-linearity of 9.5 %. The advantage of the channel configuration presented in 6.2-a (i.e. with NMOS switch) is good linearity of the transfer characteristic for low input signals. However, the dynamic range of this structure is limited by the threshold voltage of the NMOS transistor acting as the row selection switch. In turn, the second channel configuration illustrated in figure 6.2 (i.e. with transmission gate) offers wider dynamic range, but it is characterized by worse linearity. It is expected that the reason of the poor linearity is asymmetry of the characteristic of the transmission gate due to its design according to inappropriate transistor models. This conclusion was exploited in the design of later prototypes of the SOI sensor.

6.2 Large-Scale Prototypes of SOI Sensors

Measurements of the small-area monolithic active pixel sensors realized in silicon on insulator technology allowed preliminary validation of the concept of the new device. After this feasibility study, larger-area and completely functional prototypes of the SOI detectors were designed. The configuration of these sensors was imposed by the requirements of imaging applications in terms of measurement of the integrated charge, large dynamic range, well-defined integration time and short dead time. Detailed description of the design of the real-size sensors and the tests results will be presented in the following sections.

6.2.1 Overview of Large-Scale Sensor Design

The real-size prototypes of the SOI sensors were developed in two versions. A photograph of the larger sensor, called SOIDET1, is presented in figure 6.28-a. This chip is characterized by the total dimensions of 24 mm x 24 mm and it covers the active area of 19.2 mm x 19.2 mm. The sensor consists of 128 by 128 readout channels, grouped in four functionally independent quadrants with 64 by 64 channels each. A general architecture of a single quadrant of the chip is presented in figure 6.29. Every quadrant has its own set of the biasing and control lines and its own analogue signal output. Such a solution allows using at least part of the detector in the case of defects in other areas of the structure. It also increases the readout speed by enabling parallel

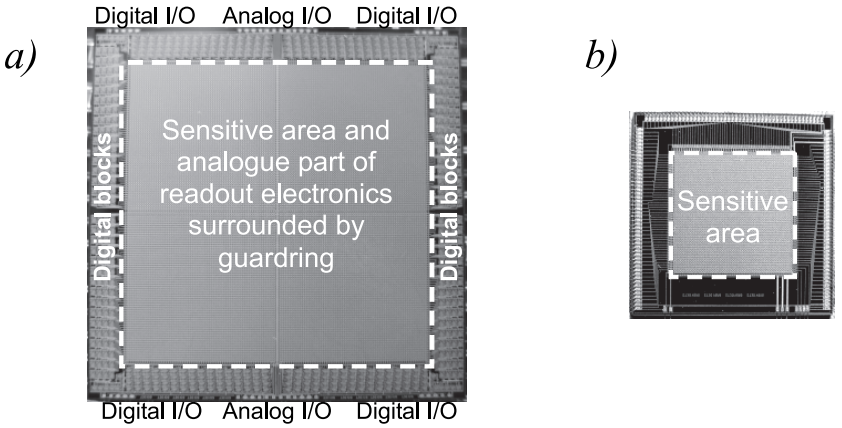


Figure 6.28: Photographs of the large-scale SOI sensor prototypes: a) SOIDET1 sensor with 128 x 128 channels and integrated digital control blocks, b) SOIDET2 sensor with 48 x 48 channels.

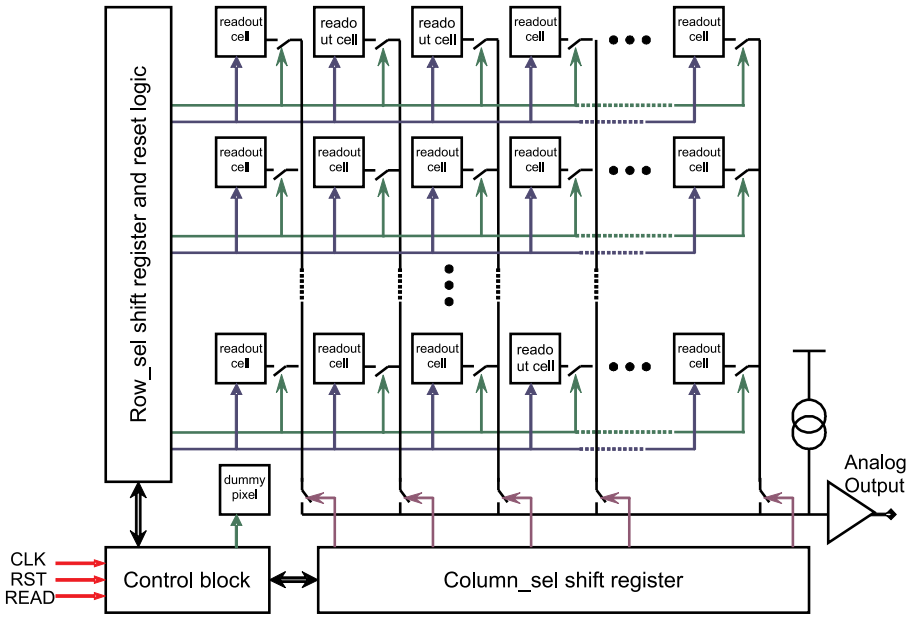


Figure 6.29: General architecture of the front-end electronics implemented on the SOIDET1 detector.

operation and gives compatibility with the SUCIMA Imager DAQ system [105]. Since all the peripheral elements of the readout circuit, as well as the detector guardrings, are designed only along two neighbouring sides of the quadrants, there is no dead area between the detector segments. The input/output pins of the sensor are placed at the top and bottom sides of the chip, which also allows building longer detector ladders with small dead areas between the chips.

The smaller sensor, called SOIDET2, is similar to the described above one, but its readout matrix consists of only single array of 48 by 48 cells. This sensor has the active area of 7.2 mm x 7.2 mm, which corresponds to the total chip dimensions of 12 mm x 12 mm. On the contrary to the larger sensor, the smaller prototype does not have any implemented on-chip digital control blocks, and thus, it requires external circuits for the readout supervision. A photograph of the SOIDET2 detector is depicted in figure 6.28-b.

Design of Analogue Part

Like in the case of the small test sensors, the main components of the analogue parts of the SOIDET1 and SOIDET2 detectors are matrices of active cells, consisting of pixel diodes monolithically coupled to their readout channels. In view of the requirement of the integrated charge measurement and the relatively large minimum feature size of

the IET process (3 μm), the readout cell solution presented in figure 6.2-b is preserved in the design of the real-size prototypes of the SOI sensor. Some minor modifications are introduced in order to adjust the sensor layout to revised design rules provided by the manufacturer. Additionally, the polysilicon-metal1 capacitor C_{cap} is removed since the new design rules translate into larger parasitic capacitance at the input node. For enhancement of the sensor sensitivity, the area of the protecting diode is reduced to 324 μm^2. At last, the width of the PMOS transistor in the transmission gate forming the row selection switch is increased from 10 μm to 15 μm in order to improve the linearity of the front-end electronics. As the result, the dimensions of a single cell of 150 μm x 150 μm are achieved for the large-scale SOI sensors. The final layout of the detector channel implemented on the SOIDET1 and SOIDET2 chips is presented in figure 6.30.

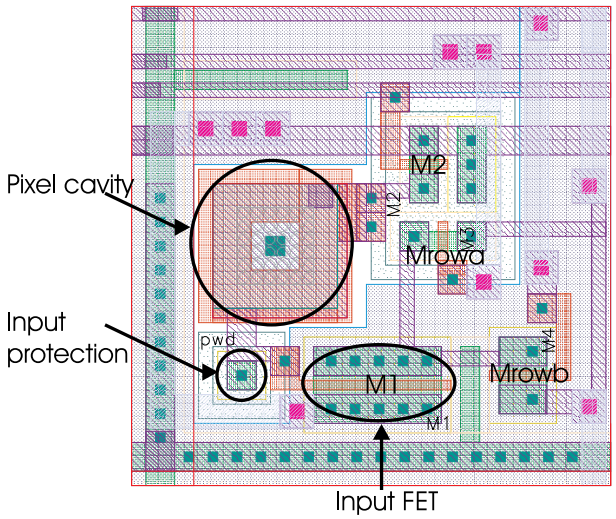


Figure 6.30: Layout of a single cell of the large-scale prototype of the SOI sensor.

Apart of the readout matrix, the analogue part of the SOI sensor prototypes contains:

- Common current source (with dimensions of $W/L = 30\mu\text{m}/20\mu\text{m}$) acting as an active load of the source followers building sensor cells
- Output buffer in the form of an NMOS source follower
- "Dummy pixel", which is a cell without the detecting diode

The latest element is selected whenever none of the active cells is read out. It keeps the current source permanently active and reduces the time required to set up a valid value of the signal at the output of the sensor.

In the design of the active matrices of the real-size SOI sensors, a special effort was put in minimizing: the crosstalk between neighbouring cells, the interaction between the readout and radiation sensitive parts of the SOI sensor and the interferences induced by the operation of digital blocks. As illustrated in figure 6.30, neighbouring cells of the sensor active matrix are separated by an n^+ region implanted in the device layer and connected to the positive supply voltage. Such a solution not only abates the coupling between the adjacent channels, but also decreases the bulk sheet resistance between the nodes of the electronics circuit and the voltage supply line. As discussed in section 4.4, it translates into the reduction of the crosstalk between the radiation sensitive substrate and the readout electronics. For further minimizing of the interaction between the readout and detecting part of the sensor, the row selection and inverted row selection lines are routed to the particular cells at the nearest distance allowed by the layout design rules. These lines are also led in parallel to the contact to the electronics bulk.

The switching noise coming from the digital part of the sensor is reduced by the proper configuration of the guardring around the detector diodes. Taking advantage of the fact that in the SOI technology, creating the guardring in the handle wafer requires etching-down the device layer, the crosstalk between the sensitive substrate and the digital electronics, as well as the crosstalk between the analogue and digital parts of the readout circuit can be minimized by manufacturing all the analogue elements of the chip inside the guardring and all the digital blocks outside the guardring. This solution is schematically illustrated in figure 6.31-a. However, the separation of the analogue active matrix from the digital control blocks by the detector guardring requires routing the digital control lines over deep trenches. For this reason, the guardring layout presented in figure 6.31-b has been proposed. It has the form of elongated pixels connected by a common biasing line (metallization level 1). The sets of the signal lines are led to the particular rows and columns of the readout matrix by the second metallization layer. Although such a solution does not ensure complete separation of the substrates of the digital and analogue parts of the front-end electronics, it should still significantly reduce the influence of the switching noise on the sensor operation.

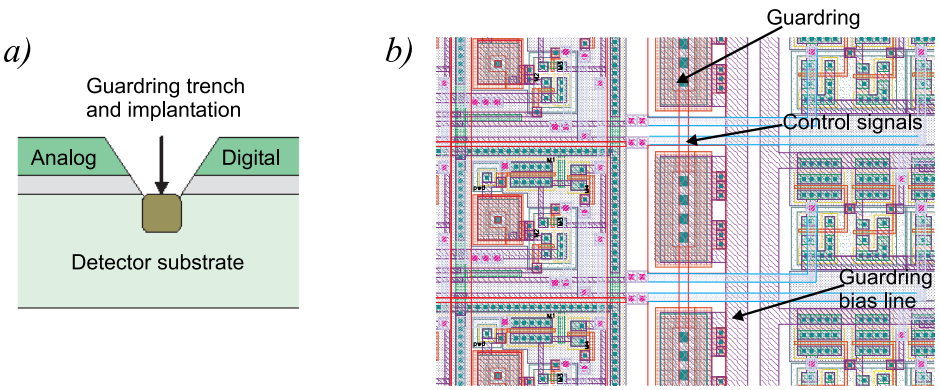


Figure 6.31: a) Separation of the analogue and digital parts of the front-end electronics by a guardring trench; b) layout of the detector guardring.

Design of Digital Part

The digital part of the SOIDET2 chip is restricted to a set of inverters and buffers, required for the formation of the "direct" and "inverted" signals steering the cell selection switches. In turn, the digital electronics of the SOIDET1 sensor is a more complex system, which provides the generation of all the internal signals needed to access particular channels of the active sensor. The digital part of a single quadrant of the SOIDET2 chip is constituted by a column selection register, a row selection register integrated with a reset selection logic and a control block responsible for the readout initialisation and supervision. For the proper operation of the digital electronics, only three external signals are required: "READ", "CLK" and "RST".

The readout of the SOIDET1 sensor is initialized when a high level on the "READ" line is sampled by a falling edge of the "CLOCK" signal. It can be restarted at any moment by activating the asynchronous "RST" signal. The implemented readout method relies on a classical serial organisation. In order to guarantee short sensor dead time and well-defined integration time, which are required for medical imaging applications, a new readout sequence was developed for the real-size SOI sensor. This solution (presented in figure 6.32) is in principle similar to the rolling shutter technique [107], where the rows of the readout matrix are both reset and read out (after the integration time) one by one in the same sequence and at the same speed. In contrast to this traditional technique, during the proposed readout sequence, every channel is accessed twice: immediately after the reset of the diode and after the integration time, which is equal to the readout time of the whole matrix. The double sampling provided

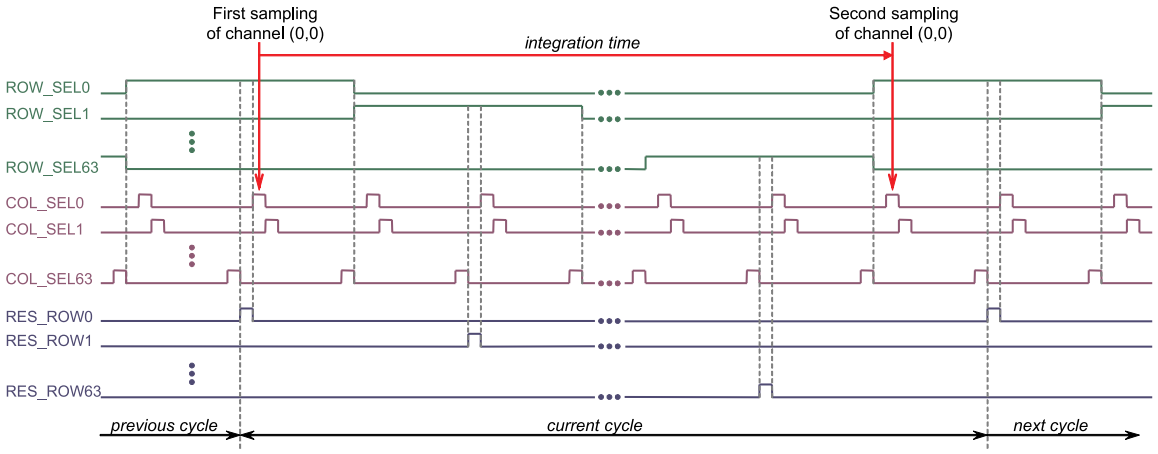


Figure 6.32: Readout sequence implemented on real-size prototypes of the SOI sensor.

during the readout sequence enables external correlated double sampling processing. The time period between both samples is exactly the same for every channel of the readout matrix, and thus, the charge integration time is defined very precisely. The sensor dead time is very short - below 1 % with reference to the integration time - because during the readout of one channel, the others continue the charge integration and the channel reset is performed "on the run". The described method does not require any additional elements of the readout channel, which allows minimizing the cell dimensions. The price to be paid is increased by a factor of 2 readout time or clock frequency.

6.2.2 Evaluation of Charge-to-Voltage Conversion Gain and Equivalent Noise Charge

Due to the modifications of the readout channel and the presence of the additional output stage, the expected charge-to-voltage conversion gain and the equivalent noise charge have to be recomputed for the large scale SOI sensor prototypes. Assuming the same working conditions of the input transistor of the readout channel (indicated by M1 in figure 6.2-b) as for the small-area sensors, the change of the conversion gain is mainly the result of the different value of the integrating capacitance. Since the follower transistor of the output buffer operates at zero bulk-source voltage, the gain of this stage does not change significantly the charge-to-voltage conversion ratio of the designed real-size SOI sensors, though it contributes to the total noise.

To estimate the new value of the sensor gain, several components of the integrating capacitance have to be recalculated - the junction capacitance of the pixel diode C_{det}, the junction capacitance of the protection diode C_{prot} and the parasitic capacitance of the interconnection between the pixel diode and the input of the readout channel C_{inter}. Following the same procedure like in section 6.1.2, one obtains the values of the particular contributions to the total integrating capacitance summarized in table 6.3. The numbers given in the table are evaluated assuming zero input voltage and the nominal value of the device layer thickness. The values of the total integrating capacitance C_{int} as a function of the device layer thickness and the input voltage are plotted in figure 6.33. As presented, the integrating capacitance equals approximately

$$C_{int} = 252.8 \text{ fF}$$

and it varies by 5.1 % for the input voltage range of 0 V to 3.5 V. Despite removing the additional polysilicon-metal1 capacitor C_{cap}, the total capacitance seen from the

Table 6.3: Contribution of the particular capacitances to the total integrating capacitance seen at the input node of a cell of the SOIDET1 and SOIDET2 sensors. Junction capacitances are calculated for zero voltage at the input node.

	C_{cap}	C_{det}	C_{prot}	C_{insf}	C_{res}	C_{cav}	C_{inter}
Area [μm^2]	0	22500	324	-	-	1061	-
Value [fF]	0.0	5.9	20.1	29.4	67.6	104.5	38.3

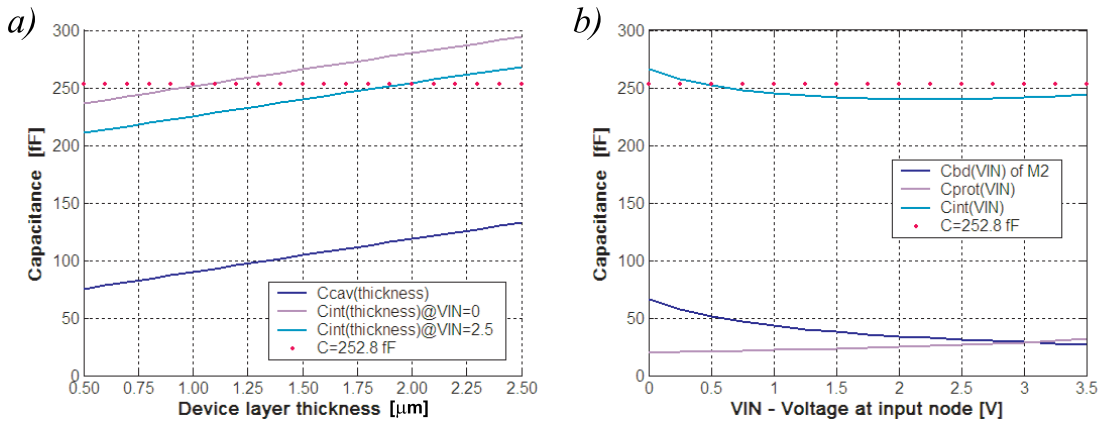


Figure 6.33: a) C_{int} as a function of the device layer thickness and b) C_{int} as a function of the voltage level at the input of readout channel.

input of the readout channel slightly increased in comparison with the small area SOI detectors. This is result of the mentioned new design rules that required longer interconnection lines.

After taking into account the characteristics given in figures 6.33 and 6.7, one obtains the values of the charge-to-voltage conversion gain as a function of the input voltage given in figure 6.34. The nominal value of the conversion gain of:

$$G_{Q\rightarrow V} = 3.50 \text{ mV/fC}$$

is calculated. This corresponds to the following value of the charge-to-voltage conversion gain referred to the number of the collected charge carriers:

$$G_{N_q\rightarrow V} = 0.56 \ \mu\text{V/e}^-$$

As given in figure 6.34, this value changes by 4.9 % when the voltage at the input node ranges from 0 V to 3.5 V.

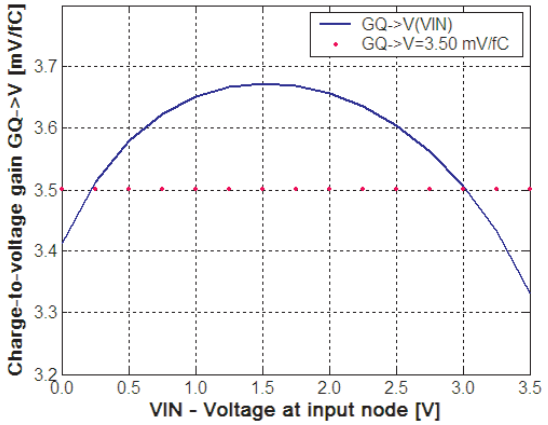


Figure 6.34: Estimated charge-to-voltage gain of the large-scale SOI detectors as a function of the input voltage.

Different values of the integrating capacitance and the conversion gain influence also the equivalent noise charge of the large-scale SOI sensors. Other factors that change the value of the ENC in comparison with the test structures are: increased capacitance of the column and output lines, different value of the integration time and characteristics of the output stage.

The equivalent noise charge generated during the reset phase ENC_{res} can be calculated by putting into the equation 6.21 the new value of the integrating capacitance at zero input voltage. For $C_{int}(0V)$ of approximately 265.8 fC, one immediately obtains the ENC_{res} of 206 e^-.

Computing the ENC generated during the integration phase requires the estimation of the integration times for the SOIDET detectors. Taking into consideration the readout sequence implemented on the SOIDET1 chip (figure 6.32), the following relation between the readout clock period T_{clk} and the integration time t_{int} can be found:

$$t_{int} = (2size^2 + size - 1)T_{clk} \tag{6.39}$$

where $size$ is the number of columns or rows in a single quadrant of the SOIDET1 detector (i.e. $size = 64$). The integration time of the SOIDET2 detector depends on the readout sequence implemented in the external control electronics. If the readout method is the same as in the case of SOIDET1 chip, the integration time can be calculated relying on the equation 6.39, but the different size of the active matrix has to be taken into account (i.e. $size = 48$). Alternatively, if the readout method presented in figure 6.19 is applied, the integration time can be computed as:

$$t_{int} = [(size + 1)size]T_{clk} \tag{6.40}$$

A general expression of the ENC_{int} as the function of the clock period may be derived by putting one of the last two equations into formula 6.23. On supposition of the leakage currents of order of 200 nA/cm^2, the obtained values of the equivalent noise charge due to the integration phase for different clock frequencies are summarized in table 6.4. As presented, if the readout sequence presented in figure 6.32 is used, the clock frequency of order of 10 MHz is necessary to achieve reasonable noise performance of the large-scale prototypes for the assumed leakage currents.

Table 6.4: ENC due to the integration phase for the large-scale SOI detectors at different readout clock frequencies f_{clk} and on the assumption of th leakage currents of 200 nA/cm^2.

Readout sequence	according to fig. 6.32						fig. 6.19		
Sensor	SOIDET1			SOIDET2			SOIDET2		
$\mathbf{f_{clk}}$ [MHz]	1	4	10	1	4	10	1	4	10
$\mathbf{t_{int}}$ [ms]	8.26	2.06	0.83	4.66	1.16	0.47	2.35	0.59	0.24
$\mathbf{ENC_{int}}$ [e$^-$]	1523	761	482	1144	572	362	813	406	257

The thermal noise contributed by the input follower transistor (M1 in figure 6.2-b), the cell selection switches and the common current source (M3 in figure 6.5) can be evaluated basing on equations 6.25-6.30. Assuming the same operating point as in the case the small test sensors, only the load capacitance C_L has to be recalculated to estimate the value of the equivalent noise charge generated by active cells during the readout phase. Considering the layout of the sensor active matrix, the load capacitances of 8.4 pF and 6.4 pF are estimated for the SOIDET1 and SOIDET2 chips, respectively. This translates into $ENC_{t,read}$ of approximately 56 e^- for the larger prototype and 64 e^- for the smaller one.

In order to complete the noise analysis of the SOIDET1 and SOIDET2 sensors, the performance of the output buffer has to be addressed. Since the buffer distinguishes by the wide bandwidth (about 12 MHz) and the gain close to unity, it does not influence the noise contributed by the input stage of the readout circuit, but it is a source of additional noise. To calculate the output referred r.m.s. thermal noise voltage of this stage, the schema and the noise model presented in figure 6.35 has to be studied. One obtains the following equations describing the output referred mean square noise voltages due to the M4 and M5 transistors, respectively:

$$\overline{V^2_{n,t,M4}} = \int_0^\infty 4kTn\frac{2}{3}\frac{1}{g_{m4}}\frac{1}{1+\left(2\pi f\frac{C_{LBUF}}{g_{m4}}\right)^2}df = n\frac{2}{3}\frac{kT}{C_{LBUF}} \approx 1.2\frac{kT}{C_{LBUF}} \tag{6.41}$$

$$\overline{V^2_{n,t,M5}} = \int_0^\infty 4kTn\frac{2}{3}\frac{g_{m5}}{g^2_{m4}}\frac{1}{1+\left(2\pi f\frac{C_{LBUF}}{g_{m4}}\right)^2}df = n\frac{2}{3}\frac{kT}{C_{LBUF}}\frac{g_{m5}}{g_{m4}} \approx 1.2\frac{kT}{C_{LBUF}}\frac{g_{m5}}{g_{m4}} \tag{6.42}$$

where g_{m4} and g_{m5} are the transconductances of the M4 and M5 transistors and C_{LBUF} is a load capacitance consisting of the output pad capacitance ($\approx$ 300 fF) and the input capacitance of the external electronics conected to the output of the sensor ($\approx$ 2 pF). As given by the above formulas, the output referred mean square noise voltage associated with the thermal noise depends only on the load capacitance C_{LBUF} and the ratio of the g_{m5} and g_{m4} tranconductances, which equals 0.335. Thus, after taking into consideration the calculated earlier charge-to-voltage conversion ratio of 0.56 μV/e^-, the equivalent noise charge due to the buffer thermal noise $ENC_{t,out}$ of 95 e^- is easily obtained.

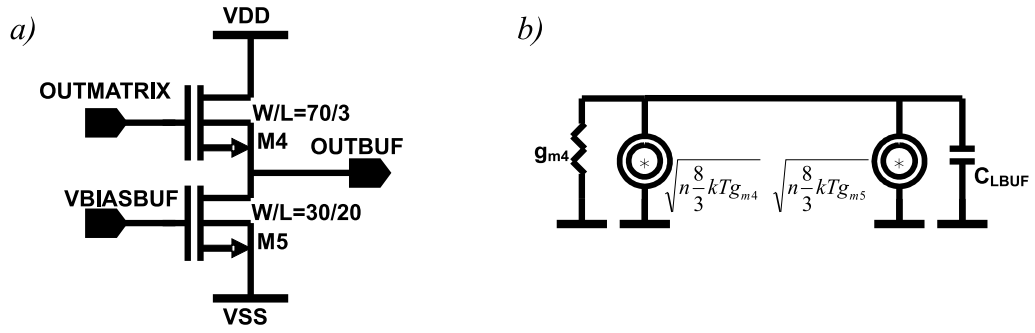


Figure 6.35: a)Schematic view and b) simplified noise model of the output stage of the large-scale SOI sensor prototypes.

Since NMOS transistors are typicaly characterized by higher flicker (1/f) noise, the equivalent noise charge $ENC_{f,out}$ associated with this noise source has to be also examined for the output stage. For this purpose, the schematic diagram similar to 6.35-b may be used, but the thermal noise sources should be replaced by the flicker noise generators with the power spectral density expressed by equation 6.16. In such a way, the following integrals describing the total output referred mean square noise voltage associated with the flicker noise of the transistors M4 and M5 are derived:

$$\overline{V^2_{n,f,M4}} = \int_0^\infty \frac{\mathrm{KF} I_D^{\mathrm{AF}}}{f^{\mathrm{EF}} C_{ox} L^2_{M4} g^2_{m4}} \frac{1}{1+\left(2\pi f \frac{C_{LBUF}}{g_{m4}}\right)^2} df \tag{6.43}$$

$$\overline{V^2_{n,f,M5}} = \int_0^\infty \frac{\mathrm{KF} I_D^{\mathrm{AF}}}{f^{\mathrm{EF}} C_{ox} L^2_{M5} g^2_{m5}} \frac{1}{1+\left(2\pi f \frac{C_{LBUF}}{g_{m4}}\right)^2} df \tag{6.44}$$

where L_{M4} and L_{M5} are the channel lengths of the M4 and M5 trasistors, respectively, and I_D is the output buffer current of 20 μA. Using of the symbolic math toolbox implemented in the Matlab package [106] and putting into the above integrals the noise model parameters (KF, AF and EF) reporoted for the IET-SOI technology in [98], the total $ENC_{f,out}$ of 101 e^- is computed.

The obtained results of the noise analysis of the readout channel (during reset, integration and readout phases) and the output follower allow calculation of the total equivalent noise charge ENC_{tot} of the large-scale SOI sensor prototypes. The final result depends on the readout clock frequency and some parameters that may vary from one lot to another. Assuming the leakage currents of 200 nA/cm^2 and the integration time of approximately 2 ms, the ENC_{tot} of 803 e^- is obtained at room temperature.

This relatively high equivalent noise charge is dominated by the noise generated during the integration phase. Therefore, in order to improve the noise performance of the large-scale SOI sensors, shorter integration time or significant reduction of the leakage currents are required.

6.2.3 Measurements of Large-Scale SOI Sensors

Like in the case of the small-are test structures of SOI sensors, the performance of the large-scale prototypes was verified experimentally. Due to the complexity of the sensor designs, the measurements were performed in several steps. First, the waveforms at the output of particular channels of the SUCIMA2 detector were observed and the correctness of the readout sequence was tested for the SUCIMA1 chip. Afterwards, the sensor response to minimum ionising electrons was examined. One of the prototypes of the large-scale SOI sensors was also used for imaging with the usage of soft X-rays.

For the purpose of the characterization of the large-scale SOI sensors, both types of the prototypes were bonded to dedicated printed circuit boards and tested with the usage of the SUCIMA Imager DAQ system. In order to amplify the sensor output signals and adjust the voltage levels, the external analogue circuitry illustrated in figure 6.20 was implemented on the test boards along with the detector structures. In compatibility with the sensor designs, the PCBs for the SUCIMA1 detectors consisted of four analogue interfaces for the parallel readout of four quadrants of the chip. In turn, the PCBs for the SUCIMA2 detectors consisted of only one analogue interface. Since the design of the smaller detectors did not include digital control blocks, the readout supervision for these chips was provided externally by a CPLD Xilinx programmable chip from the XC95288 family. Photographs of the boards are presented in figure 6.36.

Observation of Charge Integration

The measurements of the full-size SOI detectors were started from the SOIDET2 prototype. The external readout control for this chip allowed selecting a single channel and examining the corresponding output waveform with a digital oscilloscope. In such a way, the charge integration process could be observed.

Exemplary output waveforms obtained for one of the channels of the SOIDET2 sensor are presented in figure 6.37. The left plot illustrates the integration of the detector leakage current for different bias voltages applied to the detector backplane, while the right plot shows the detector response to the red light of a laser pointer.

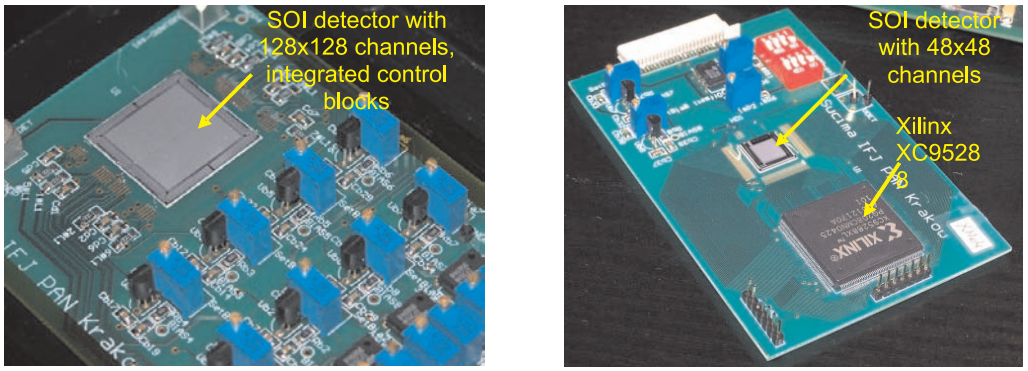


Figure 6.36: PCBs for the tests of the large-scale SOI detectors – for the test of the detector with 128x128 readout channels (left) and the detector with 48x48 readout channels (right).

The results were obtained for the integration time set at 3.5 ms by a periodic and simultaneous reset of all the channels of the sensor. As expected, the leakage current dependence on the detector reverse bias and the detector sensitivity to the light were observed. Proper operation of the analogue electronics and the linear response of the sensor for the output voltage up to approximately 1.75 V were also demonstrated.

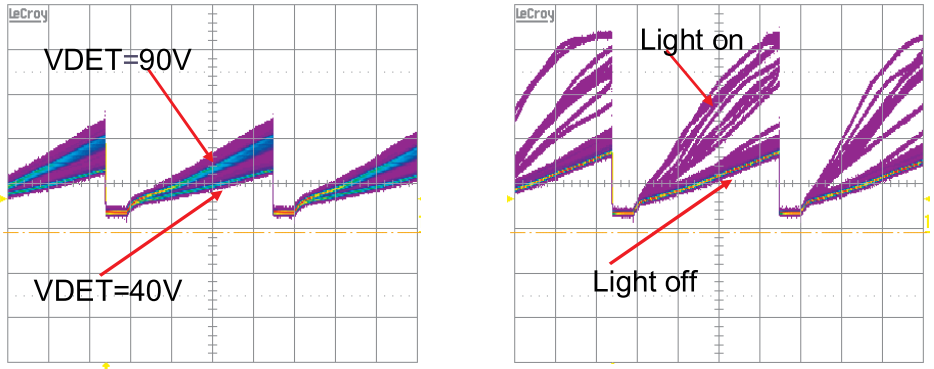


Figure 6.37: Output waveforms for one of the channels of the SOIDET2 detector obtained for different detector bias (left) and for the detector exposed and not exposed to the red light of a laser pointer (right). Time base settings - 1 ms per division, vertical resolution - 0.5 V per division.

Readout Tests of SOIDET1 Sensor

Other introductory tests of the large-scale SOI sensors concerned the functionality of the digital control electronics implemented on the fully integrated SOIDET1 chip. In order to examine the correctness of the readout sequence, laser pointer light was shinned on different quadrants of the tested detectors and the readout results (after performed on-line CDS processing and pedestal subtraction) were observed on a GUI panel. The measurements were performed for the readout frequencies from 125 kHz to 10 MHz. The tests revealed serious problems with the production yield of the largest prototypes of the proposed monolithic sensors realized in SOI technology. Some of the tested chips exhibited the short circuit between the device layer and the p^+ pixel implantations that had been observed during the wafer level tests of the SUCIMA2 test structure. Only two of ten tested chips displayed partial proper operation of the digital electronics. First sensor showed proper functionality of one quadrant of the readout matrix up to the frequency of 125 kHz. In view of the significant number of the readout cells of the SOIDET1 chip and the correlation between the readout time and the integration time, this readout clock frequency was too low to achieve good noise performance of the sensor and to avoid its saturation. Second partially functional sensor showed proper generation of the readout sequence for three quadrants up to the frequency of 10 MHz. The visualizations of the readout results for this sensor are presented in figure 6.38. The spot shape of the laser pointer can be easily distinguished at two different positions, which proves the proper design of the digital control blocks. However, the presented results were obtained by shinning the electronics side of the sensor. No signal was observed while shinning the backplane of the chip. This indicated the detector insensitivity to ionising radiation. For this reason, further tests of the large-scale prototypes were performed with the use of the SOIDET2 structures.

The observed problems with the production yield of the SOIDET1 sensors can be justified by the significant dimensions of the structure and the complexity of the mixed-mode design. The SOIDET1 sensor is more sensitive to the processing faults than the SOIDET2 sensor since an incorrect characteristic of one transistor of the digital electronics may cause the dysfunction of the entire chip. It should be also pointed out that, unlike the hybrid detectors, the monolithic active pixel sensors require simultaneously a high quality of the detector sensitive substrate and the proper operation of the readout electronics. Additionally, the areas of the detector structures usually exceed the typical sizes of conventional integrated circuits.

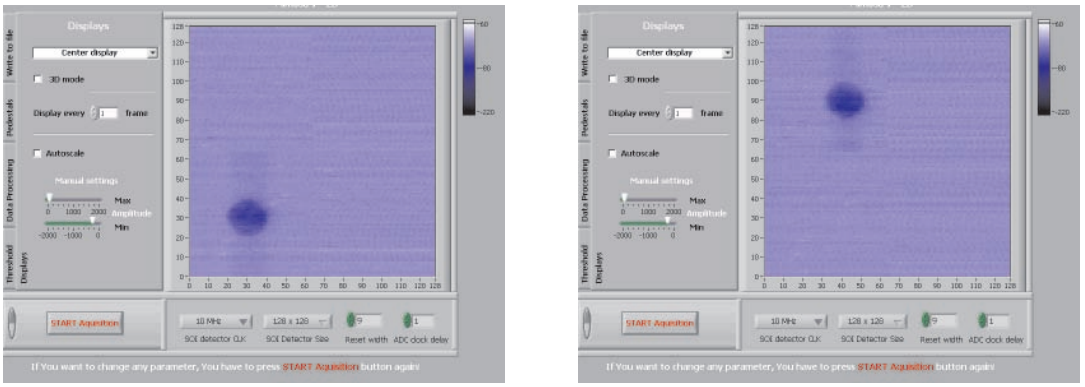


Figure 6.38: Visualization of the readout results obtained with the SOIDET1 detector and laser pointer light shined on two different quadrants of the readout matrix.

Estimation of Leakage Current

The junctions quality of the large-scale SOI sensors was examined by the measurements of the detector leakage currents of the best SOIDET2 chip. These measurements were performed using the indirect method that based on the equation 6.38 and the estimated value of charge-to-voltage conversion gain. The tests were carried on at room temperature and the reverse bias voltage above full depletion of the detector substrate (70 V). The integration time t_{int} was set at 2.35 mV and the total collected charge was computed by measuring the sensor output signal after the CDS processing.

The distribution of the leakage current per square centimetre obtained for the whole matrix of the SOIDET2 sensor is given in figure 6.39. As presented, the typical

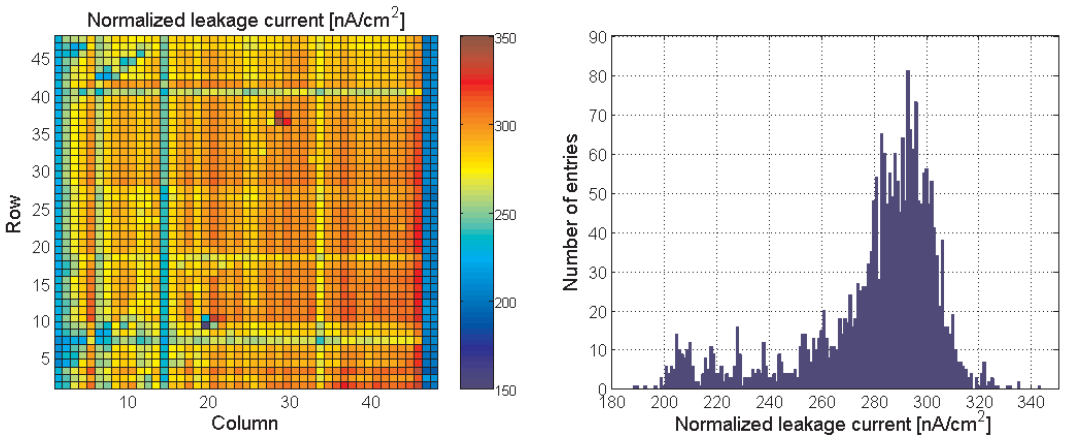


Figure 6.39: Distribution of the normalized leakage current per square centimeter for one of the SOIDET2 chips. Results obtained at temperature of 23 °C and the detector reverse voltage of 70 V.

normalized leakage current of order of:

$$I_{leak} = 290 \text{ nA/cm}^2$$

was measured for the investigated sensor. This value is similar to the one achieved for the first test structures of the monolithic active pixel sensor realized in SOI technology.

Sensor Response to Minimum Ionising Electrons

In order to examine the detecting properties of the real-size prototypes of monolithic active pixel sensors realized in SOI technology, the response of the SOIDET2 chip to MIP-like particles was measured. Like for the small-area test structures, this test was performed with the use of an uncollimated Strontium-90 beta source. During these tests, the sensor backplane was biased with 115 V to achieve full depletion of the detector substrate. Output signal was amplified before the digitisation by a factor of 2.5 to reduce the influence of external noise sources. Since achieving short dead-time was not crucial for the considered measurements, the readout scheme presented in figure 6.19 was implemented in the CPLD chip. The readout frequency of the sensor was set at 1 MHz, which corresponded to the integration time of 2.35 ms. No CDS processing was performed due to the dominating contribution of the noise generated during the integration phase. The measurement results were processed according to the scheme presented in figure 6.22. The r.m.s. noise of order of 1.5 ADC counts per pixel was obtained after the common mode suppression for the sensor connected to the DAQ system.

The sensor response to the MIP-like particles along with the pedestal distribution measured for an exemplary good pixel is presented in figure 6.40. Like in the case of the test structures of the SOI detector, the signal distribution similar to the Landau distribution was obtained after the cluster calculation. The most probably cluster pulse height of 31 ADC counts was found, which corresponded to the sensor output voltage of 12.4 mV. Taking into account the estimated charge-to-voltage conversion gain of the SOIDET2 chip, the given voltage translates into the following value of the most probable charge collected on the sensor electrode after the passage of a beta particle emitted by the Sr-90 source:

$$MIP\ charge = 22140 \text{ e}^-$$

Thw obtained results show the sensitivity of the large-scale prototype of the SOI sensor to MIP particles. With reference to the small-area test structures, higher MIP

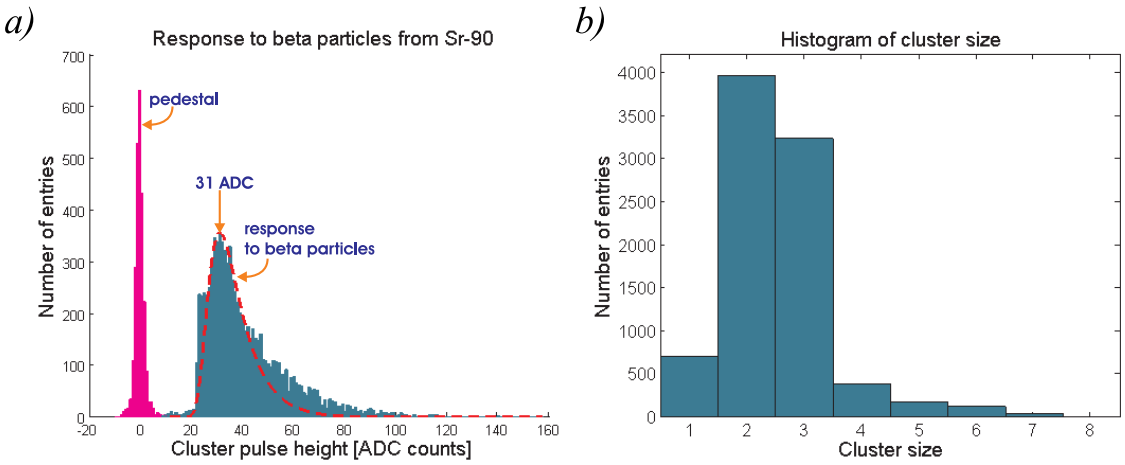


Figure 6.40: Measurement results of the sensor response to beta particles emitted by the Sr-90 source: a) histogram of the pedestal distribution after the subtraction of its average value (pink bars), histogram of the cluster pulse height measured after the exposition to beta radiation from the Sr-90 source (turquoise bars) and the Landau fit (red line); b) histogram of the cluster size.

signal was achieved with the use of the SOIDET2 sensor, but worse signal-to-noise ratio was obtained due to longer integration time. The equivalent noise charge of 1071 e^- was measured for the sensor connected to the readout system. Taking into account the noise of the acquisition system, this corresponds to the following ENC of the sensor itself:

$$ENC = 800 \text{ e}^-$$

Above value is comparable with the previous estimation.

Example of X-ray imaging

Since one of the future applications of the monolithic detectors realized in silicon on insulator technology may be the detection of low energy X-rays in medical diagnostics or diffractometery, a simple experiment, which showed imaging properties of the new device, was also performed. For this purpose, the SOIDET2 sensor was exposed to the Cu K_α radiation generated by an X-ray tube of a laboratory diffractometer.

The test set-up is presented in figure 6.41. The SOI detector was mounted at the arm of the HZG 4 diffractometer. A collimator with a rectangular (0.44 mm wide and 0.35 mm high) slit was placed between the x-ray tube and the sensor. The diffractometer tube was operated at the voltage of 30 kV and the current of 27 mA.

The reverse bias voltage of 70 V was applied to the detector backplane and the gain of the external amplifier was set at 2. No CDS processing was performed and the readout scheme presented in figure 6.19 was exploited. The readout clock frequency was set at 10 MHz to reduce the integration time. As this frequency was higher than the 3-dB cut-off frequency of the readout electronics and the adopting board, some image blurring was observed, but the noise performance of the sensor was improved.

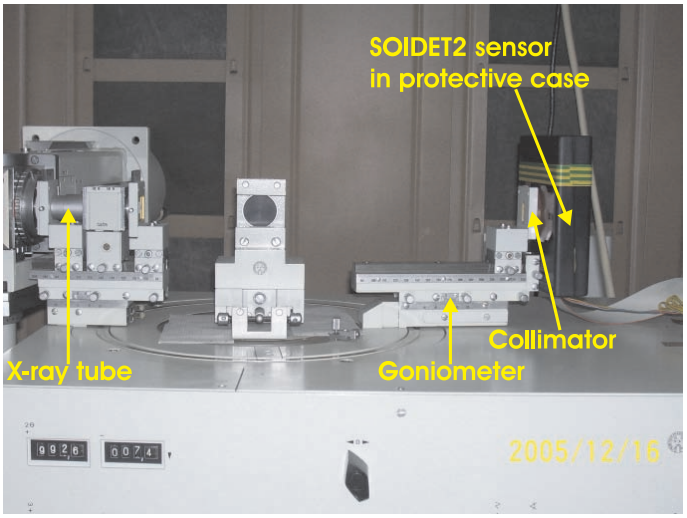


Figure 6.41: Experimental set-up used for X-ray imaging: the HZG 4 diffractometer and the SOIDET2 sensor.

The signal measured by the SOIDET2 chip was processed and transferred to the computer with the usage of the same data acquisition system as in the previous experiments. 500 frames were collected before and after switching on the x-ray tube. The image was computed as the difference of the averaged values of these two signals. For noisy and leaky pixels, characterized by the r.m.s. noise higher than 4.5 ADC counts and the leakage current higher than 325 nA/cm^2, the signal was interpolated as the mean value of the signals measured on the neighbouring cells.

The acquired image is presented in figure 6.42-a. Despite the low value of the signal, the distinct shape of the slit is visible. The average signal of approximately 10 ADC counts is measured on the fragment of the sensor covering the area of 0.45 mm x 0.3 mm. Some charge sharing on the neighbouring pixels is also observed. Figure 6.42-b shows the histogram of the measured signals before and after switching on the x-ray tube for one of the exposed pixels. As presented, the achieved signal-to-noise ratio of 10 allows distinguishing the x-ray image from the pedestal.

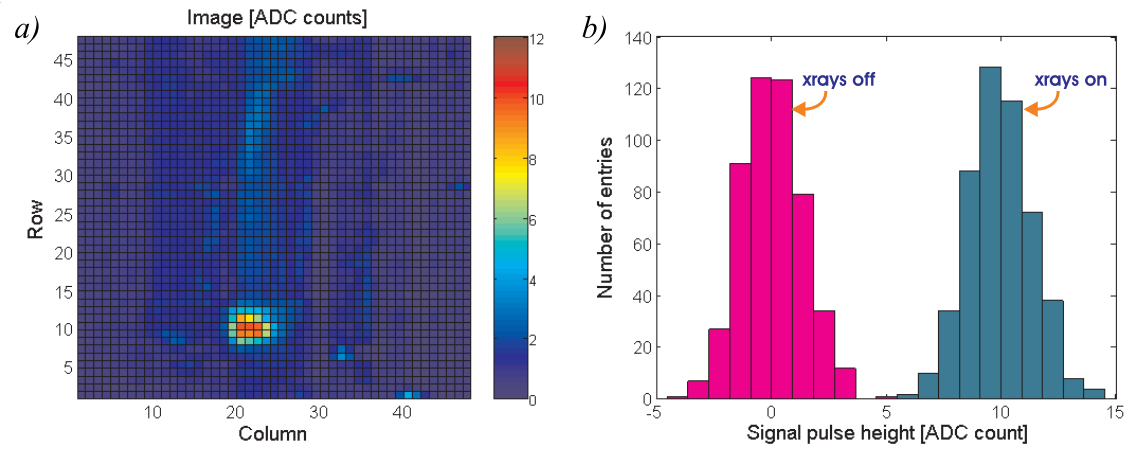


Figure 6.42: Results of soft x-rays imaging: a) image obtained after the exposition of the SOIDET2 sensor to the Cu K_α radiation; b) signal distribution obtained on the pixel located in ninth row and twenty first column, before and after switching on the x-ray tube.

The obtained results show that the SOI sensor might be used in imaging applications after an appropriate optimisation of the readout electronics. The usage of these sensors in the x-ray diffractometery would require increased value of the charge-to-voltage conversion gain because of the low x-ray energy (of order of 8 keV). The single photon counting architecture of the readout electronics is also preferred in imaging applications. The SOI technology allows fulfilling these demands but requires smaller minimum feature size of the CMOS technology used for the sensor production.

Chapter 7

Summary and Future Prospects

7.1 Summary and Final Remarks

This thesis concerns the development of a new monolithic active pixel sensor. The proposed device exploits commercially available wafer-bonded silicon on insulator substrates for the integration of a particle detector and readout electronics in one entity. The key feature of the sensor is the use of a high resistivity handle wafer as the detector sensitive material. This allows detector operation at full depletion, and consequently, efficient detection of the ionizing radiation. The tests of the prototypes of the introduced device showed that the passage of a minimum ionizing particle through the sensor active volume results in the collection of the most probable charge of approximately 20 000 electrons, which corresponds to the signal-to-noise ratio of 30. Additionally, the new sensor is characterized by manufacturing the CMOS readout electronics in a relatively thick device layer above a micrometer thick buried oxide. The performed simulations and the measurements of the sensor prototypes confirmed that such an approach allows effective reduction of the interaction between the readout electronics and the detector sensitive region formed underneath.

The realization of the new monolithic active sensor required definition of new semiconductor technology. The developed technology based on a conventional CMOS process with the minimum feature size of 3 μm. For the purpose of the technology validation, two test chips (SUCIMA1 and SUCIMA2) were designed. They allowed the characterization of the basic components of active pixels sensors, the evaluation of the mismatches of device parameters and the investigation of the performance of electronic functional blocks.

The validation and the characterization of the new sensor technology was a long lasting process that consisted of many steps. First, basic parameters of MOS transistors (e.g. threshold voltage, breakdown voltage, subthreshold currents) had to be set up, and then the matching properties of the technology could be studied. The variations of the threshold voltage and the current factor of MOS transistors and the mismatches of parallel plate capacitors were investigated. At this stage, the uniformity of the device layer thickness of the SOI wafers appeared to be a critical parameter. Although small mismatches were obtained for the devices produced on the wafers thinned down by the SmartCut process, a significant increase of the parameter variations was observed for the grinded wafers. For example, the standard deviation of the threshold voltage increased from 10 mV to 20 mV for NMOS transistors and from 10 mV to 40 mV for PMOS transistors after moving to the grinded wafers. The study of this problem indicated that it was connected with the variation of the doping concentration in the transistor bulk due to the non-uniform thickness of the device layer. As this effect was independent of the device processing and the high resistivity wafers thinned down by the SmartCut process were not available, the unavoidable parameter spread was taken into account in the design of the prototypes of the SOI sensors and in the subsequent analysis of the gathered measurements results.

As a part of the technology development, an experimental model of MOS transistors, which was subsequently used in the design of the front-end electronics of the SOI sensor, was also prepared. The approach based on the extraction of the basic Spice parameters and the measurements of the transconductance versus current and output conductance versus current characteristics. It allowed the small signal analysis and the noise optimization of the readout circuit for the SOI sensor.

After the CMOS components of the active sensor had been characterised, the processing steps of the radiation sensitive diodes were defined. The reliability of the integration of the pixel diodes and the readout channels along with the quality of the detector active substrate were studied. The measurements of the reverse characteristics of the pixel diodes indicated significant heterogeneity of the junction parameters and the leakage current of order of 200 nA/cm^2 for most of the structures. This value is an order of magnitude higher than the numbers reported for the hybrid detectors. Nevertheless, taking into the consideration the early stage of the technology development and the large number of the processing steps of the SOI sensors, this result was acceptable. It was also close to the physical limit set by the parameters of

the available SOI substrates. As the generation lifetime of 200 μs was measured for the handle layer of the SOI wafers, the leakage currents of order of hundreds nanoamps per square centimeter could be expected. Again, the performed characterisation of the charge sensitive components of the SOI sensor confirmed that one of the critical issues of the realization of the monolithic active pixels sensors in the SOI technology is the quality and the accessibility of the SOI wafers. For that reason, a joint research effort with an institute offering wafer-bonding technology has been started recently. It should allow avoiding discontinuities in the SOI sensor deliveries and preserving high quality of the handle layer of the SOI wafers during the bonding process.

The defined technology of the SOI monolithic active pixel sensors was used for the design and the production of two generations of the detector prototypes. First, small-area test structures, consisting of 8 by 8 simple readout channels (similar to three-transistor cells) were manufactured. In the design of these structures, the flexibility of the choice of the transistor types in the readout cell was exploited. In order to validate the concept of the new particle detector, the test structures of the SOI sensor were extensively examined in terms of the sensitivity to ionizing radiation, the dynamic range and the noise performance. A wide dynamic range, the charge-to-voltage conversion gain of 3.71 mV/fC and the equivalent noise charge of 560 electrons for the integration time of 420 μs were achieved.

After this preliminary feasibility study, larger-area prototypes of the SOI monolithic detectors were designed. According to the specification of the SUCIMA project, the configuration of these sensors was imposed by the requirements of imaging applications in terms of the measurement of the integrated charge, large dynamic range, well-defined integration time and short dead time. The prototypes were developed in two versions. The larger of designed sensors covered the active area of 19.2 mm x 19.2 mm. It consisted of 128 by 128 readout channels, grouped in four functionally independent quadrants. The smaller sensor was similar, but its readout matrix consisted of only single array of 48 by 48 cells. The dimensions of a single cell of both prototypes were 150 μm x 150 μm. The tests of the large-scale prototypes of the SOI sensor revealed a serious problem with the production yield, which was partially justified by the significant dimensions of the structure and the complexity of its design. For some of the tested chips, a short circuit between the electronics substrate and the pixel diodes was observed. The possible reason of the short circuit was a defect in the insulating layer between the polysilicon plate covering the pixel cavity and the device layer.

As the problem was traced, it should be avoided in the next generations of the SOI sensors. Despite the yield problems, satisfactory characteristics were observed for the best of the smaller prototypes. The sensor was characterised by the leakage current of 290 nA/cm^2, the charge-to-voltage conversion gain of 3.5 mV/fC and the equivalent noise charge 800 electrons at long integration time of 2.35 ms. Although the sensor was optimised for a high particle flux, it allowed detecting minimum ionising particles at the signal-to-noise ratio of 27.

The results of the technology characterization and the sensor prototyping allow concluding that despite some reliability problems and worse parameters of the developed SOI sensors in comparison with such mature devices as hybrid, CMOS or DEPFET sensors, the SOI technology based on the wafer-bonded substrates enable the realization of monolithic active pixel detectors with fully depleted radiation sensitive substrates. Nevertheless, further development of the proposed sensors is required in order to achieve the quality satisfactory for the imaging or tracking applications. In particular, the reproducibility of the device characteristics should be improved and the leakage currents have to be reduced.

7.2 Further Developments

Apart from the parameters variations and the relatively high detector leakage currents, a serious limitation of the existing technology of the SOI sensor is the large minimum feature size. Although it was acceptable for the basic feasibility study, it does not allow achieving the granularity necessary for most of the applications of silicon pixel detectors. For example, the vertex detector for the future linear collider requires the pixel pitch of order of 20 μm and some additional signal pre-processing integrated in the readout cell. For this reason, moving the sensor production into a deep submicron process is one of the goals of the future SOI sensor development. As a part of this research effort, the test structures sketched in appendix C have been proposed. They allow choosing the optimal and reliable construction of the connection between the detector diodes and the readout channels and assessing the quality of the junctions manufactured in the high resistivity handle wafer. The test structures exploit the possibility of the connection of the radiation sensitive diodes with the readout electronics by tiny holes in the silicon film and the BOX filled in with tungsten. Such a solution along with deep submicron CMOS processing may reduce the readout pitch

of the future SOI sensor and open the way for the implementation of the new sensor in future high energy physics experiments and other applications. It may also allow further benefiting from the SOI approach by integrating more advanced electronics in the readout cell. For instance, the photon counting mode may be implemented in the front-end electronics for the X-ray imaging applications.

Besides the efforts towards the realization of the SOI sensor in deep submicron technology, further development, basing on the existing process of the detector manufacturing, is carried on. At present, a new prototype of the sensor is being designed. The new chip is optimized in terms of the sensitivity and the low noise operation. The charge integrating capacitance is reduced by minimizing the dimensions of the interconnection lines and by either connecting the polysilicon coat over the pixel cavity to the positive supply line or removing it. As mentioned, the new configuration of the connection between the pixel diode and the readout channel should also solve the problem of the observed earlier processing fault.

For better characterization and quality control of the technology of the SOI sensor, matching properties, noise characteristics and radiation hardness of MOS devices, as well as the reverse characteristics of pixel junctions will be investigated. For this purpose, the test structures designed on the SUCIMA2 chip and summarized in appendix B will be produced in a larger quantity on the next processed wafers. Additional matrices allowing the examination of the new configurations of the pixel cavity will be tested, too.

Appendix A

Selected ISE-TCAD Models

A.1 Slotboom Band Gap Model

The effective band gap is calculated in DESSIS as a difference of the band gap at given temperature and the band gap narrowing. Band gap narrowing has the form:

$$\Delta E_g = \Delta E_g^0 + \Delta E_g^{Fermi} \tag{A.1}$$

where ΔE_g^0 is determined by the particular band gap narrowing model and ΔE_g^{Fermi} is an optional correction to account for carrier statistics. The Slotboom band gap model defines the ΔE_g^0 as:

$$\Delta E_g^0 = E_{bgn}\left[\ln\left(\frac{N_i}{N_{ref}}\right) + \sqrt{\ln^2\left(\frac{N_i}{N_{ref}}\right) + 0.5}\right] \tag{A.2}$$

Quantity N_i in above equation is the total doping concentration ($N_i = N_A + N_D$), while E_{bgn} and N_{ref} are material parameters. For silicon, the default values of the last two parameters are: $E_{bgn} = 6.92 \times 10^{-3}$ and $N_{ref} = 10^{17}$.

A.2 Masetti Doping-Dependent Mobility Model

Since in doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility, DESSIS supports models for doping-dependent mobility. In Masetti model, the doping-dependent mobility is computed as:

$$\mu_{dop} = \mu_{min1}\exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \tag{A.3}$$

where N_i is defined as in previous model and μ_{const} is low-doping reference mobility. The remaining parameters are given in table A.1 .

Table A.1: Default coefficients of the Masetti model.

Symbol	**Electrons**	**Holes**	**Unit**
μ_{min1}	52.2	44.9	$cm^2/(Vs)$
μ_{min2}	52.2	0	$cm^2/(Vs)$
μ_1	43.4	29.0	$cm^2/(Vs)$
P_c	0	9.23×10^{16}	cm^{-3}
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.34×10^{20}	6.10×10^{20}	cm^{-3}
α	0.68	0.719	-
β	2.0	2.0	-

A.3 Canali High Field Mobility Saturation Model

As the carrier drift velocity saturates in high electric fields, DESSIS supports models for the description of this effect. In Canali model, the high field mobility saturation is described as follows:

$$\mu(F) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} F}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{A.4}$$

where μ_{low} is low field mobility calculated according to the selected mobility model, v_{sat} is saturation velocity and F is driving field. At last, the parameter β depends on the temperature and is given by:

$$\beta = \beta_0 \left(\frac{T}{T_0}\right)^{\beta_{exp}} \tag{A.5}$$

where T_0 is 300 K, β_0 equals 1.109 for electrons and 1.213 for holes, and β_{exp} equals 0.66 for electrons and 0.17 for holes. The described model is valid up to 430 K.

A.4 Lombardi Mobility Degradation Model at Interfaces

The Lombardi model concerns the mobility degradation related to the high transverse electric field ($F_\perp$) at the semiconductor–insulator interface. Because of this electric field, carriers transported close to the surface are subjected to scattering by acoustic surface phonons and surface roughness. In the considered model, the surface contributions to the mobility due to acoustic phonon scattering μ_{ac} and surface roughness scattering μ_{sr} are computed in the following way:

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C\left(\frac{N_i}{N_0}\right)^\lambda}{F_\perp^{\frac{1}{3}}\left(\frac{T}{T_0}\right)^k} \tag{A.6}$$

$$\mu_{sr} = \left[\frac{\left(\frac{F_\perp}{F_{ref}}\right)^{A^*}}{\delta} + \frac{F_\perp^3}{\eta}\right]^{-1} \tag{A.7}$$

where $N_i = N_A + N_D$, $T_0 = 300$ K and $F_{ref} = 1$ V/cm. The default values of the model parameters are summarized in table A.2.

Table A.2: Default coefficients of the Lombardi model.

Symbol	**Electrons**	**Holes**	**Unit**
B	4.75×10^7	9.925×10^6	cm/s
C	5.80×10^2	2.947×10^3	$\mathrm{cm}^{5/3}/(\mathrm{V}^{2/3}\mathrm{s})$
N_0	1.0	1.0	cm^{-3}
λ	0.125	0.0317	-
k	1.0	1.0	-
δ	5.82×10^{14}	2.0546×10^{14}	$\mathrm{cm}^{-3}/(\mathrm{Vs})$
A^*	2.0	2.0	-
η	5.82×10^{30}	2.0546×10^{30}	$\mathrm{V}^2/(\mathrm{cms})$

The surface contributions to the mobility are combined with the bulk mobility μ_b according to:

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \tag{A.8}$$

The parameter D is expressed as:

$$D = \exp\left(\frac{-x}{l_{crit}}\right) \tag{A.9}$$

where x is the distance from the interface and $l_{crit} = 10^{-6}$ cm is a fit parameter.

A.5 Shockley-Read-Hall (SRH) Doping-Dependent Recombination Model

Shockley-Read-Hall (SRH) model reefers to the recombination through deep levels in the gap. The minority lifetimes required for evaluation of the recombination rate are modeled in DESSIS as a product of the doping-dependent, field-dependent and temperature-dependent factors. If the doping-dependent option is activated, the lifetime is computed as:

$$\tau_{dop}(N_i) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_i}{N_{ref}}\right)^{\gamma}} \tag{A.10}$$

where N_i is defined like in previous models and N_{ref} is $10^{16}/\text{cm}^3$. By default, the τ_{min} has zero value for both electrons and holes, while τ_{max} equals 1×10^{-5} s for electrons and $3 \times 1-^{-6}$ for holes.

Appendix B

Specification of SUCIMA1 and SUCIMA2 Chips

B.1 SUCIMA1 Test Structure

The layout of the SUCIMA1 chip is presented in figure B.1. It contains the following elements:

- E1 - Set of 5 PMOS transistors with W/L= 6/3, 25/3, 3x40/3 (different body contact geometry)
- E2 - Set of 5 PMOS transistors with W/L= 20/10, 40/20, 40/10, 20/20, 6/14
- E3 - Set of 5 NMOS transistors with W/L= 6/3, 25/3, 3x40/3 (different body contact geometry)
- E4 - Set of 5 NMOS transistors with W/L= 20/10, 40/20, 40/10, 20/20, 6/14
- E5 - Set of 3 digital gates: double load buffer, inverter and double load inverter
- E6 - Set of 2 digital gates: NAND and NOR gates
- E7 - Set of 2 common source (OS) amplifiers
- E8 - Common source – common gate (OS – OG) amplifier
- E9 - Data Flip-Flop
- E10 - Set of 13 NMOS current sources with W/L=1x100/10, 3x50/10, 1x25/10, 1x12.5/10, 1x10/10, 1x50/20, 1x25/20, 1x7.5/3, 3x15/3

- E11 - Set of 13 PMOS current sources with W/L=1x100/10, 3x50/10, 1x25/10, 1x12.5/10, 1x10/10, 1x50/20, 1x25/20, 1x7.5/3, 3x15/3
- E12 - Set of 8 couples of precise ratio capacitors
- E13 - Set of 8 couples of capacitances with values of: 10 fF, 100 fF, 1 pF, 10 pF
- E14 - 8x8 matrix of readout channels with switches in the form of transmission gates and contacts to the pixel diodes. Matrix connected to biasing circuit
- E15 - 6x5 matrix of readout channels with switches in the form of transmission gates and test signal input pads. Matrix connected to biasing circuit
- E16 - 8x8 matrix of readout channels with single-transistor switches and contacts to the pixel diodes. Matrix connected to biasing circuit
- E17 - 5x5 matrix of readout channels with single-transistor switches and test signal input pads. Matrix connected to biasing circuit

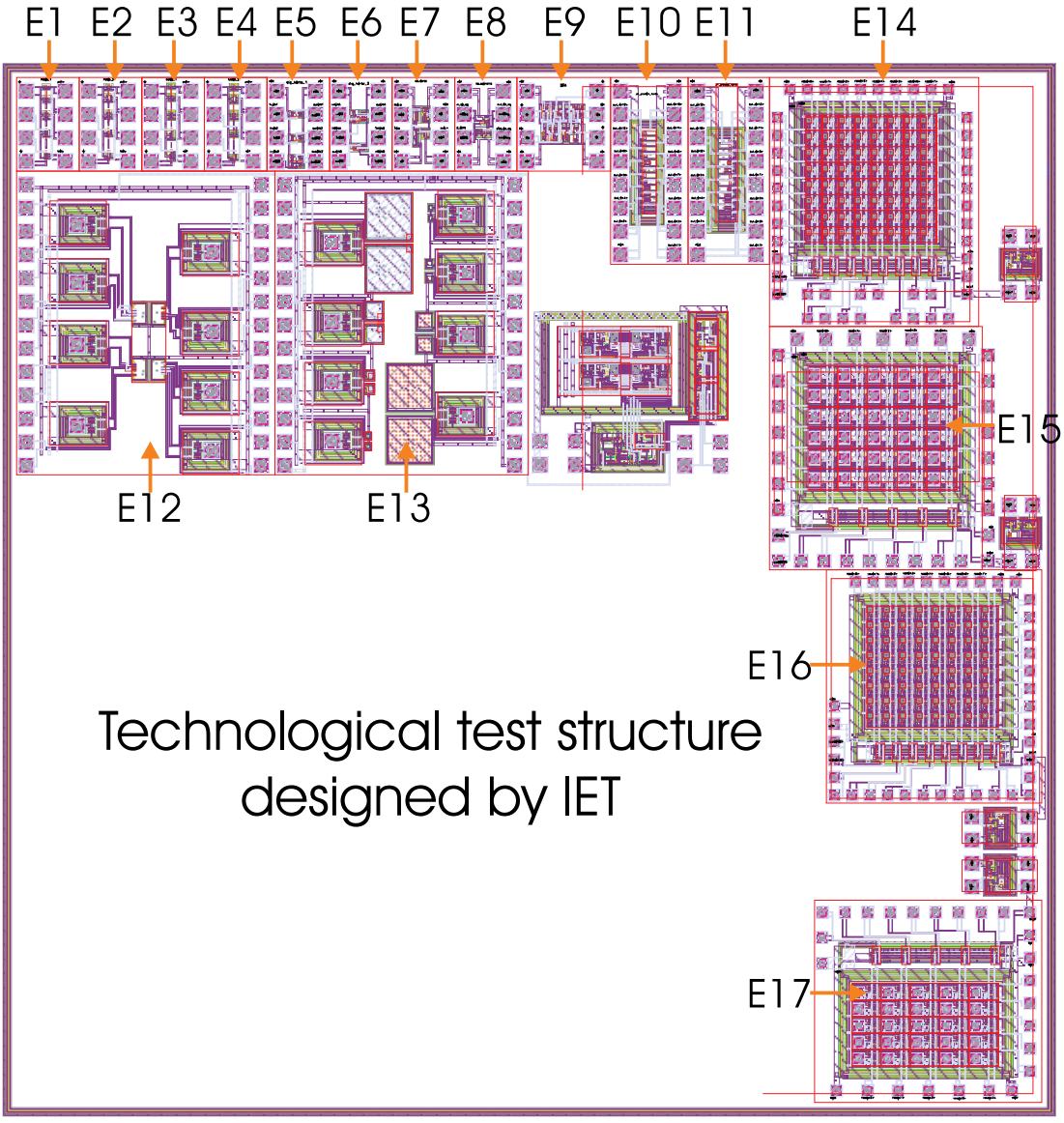


Figure B.1: General layout of the SUCIMA1 test structure.

B.2 SUCIMA2 Test Structure

The layout of the SUCIMA2 chip is presented in figure B.2. It contains the following elements:

- E1, E2, E3, E4, E5, E6, E9, E10, E11, E12, E13, E16 - Modules identical as on the SUCIMA1 chip
- F1 - Matrix of 10x10 pixels without electronics, pitch 80 μm, double guardring, additional contact to the device layer, internal pixels connected into the sets of 16 pixels, external pixels joined together
- F2 - Matrix of 10x10 pixels without electronics, pitch 150 μm, single guardring, additional contact to the device layer, internal pixels connected into the sets of 16 pixels, external pixels joined together
- F3 - Test structure for investigating matching properties of short channel NMOS transistors: 7 couples of transistors with the same and different orientation, with the symmetric and asymmetric bulk and gate polarization, the cross-coupled pairs, etc. W/L=12/3
- F4 - Test structure for investigating matching properties of long channel NMOS transistors: test structure similar like F3, but W/L=60/15
- F5 - Test structure for investigating matching properties of short channel PMOS transistors: 7 couples of transistors with the same and different orientation, with the symmetric and asymmetric bulk and gate polarization, the cross-coupled pairs, etc. W/L=12/3
- F6 - Test structure for investigating matching properties of long channel PMOS transistors: test structure similar like F5, but W/L=60/15
- F7 - Test structure for investigating noise characteristics of NMOS transistors: set of 3 NMOS transistors with W/L=1500/3 and different layouts: snake-like transistor with a bulk contact close to the source, snake-like transistor with a local bulk polarization (studies of the bulk sheet resistance contribution to the total noise), transistor with a comb gate (studies of the gate resistance contribution to the total noise)

- F8 - Test structure for investigating noise characteristics of PMOS transistors: set of 3 PMOS transistors with W/L=1500/3 and different layouts: snake-like transistor with a bulk contact close to the source, snake-like transistor with a local bulk polarization, transistor with a comb gate
- F9 - Test structure for investigating radiation hardness of NMOS transistors: set of 3 NMOS transistors with different layouts: conventional layout, H-gate and enclosed geometry
- F10 - Test structure for investigating radiation hardness: inverter with conventional layout and enclosed geometry of the NMOS transistor
- F11 - Matrix of 8x16 readout channels with a conventional CSA (charge sensitive amplifier) configuration: 8x8 channels with a standard contact and 8x8 - with reduced input capacitance, global reset and sampling and hold, auto-polarization of the feedback resistor
- F12 - Matrix of 16x16 readout channels with reduced capacitance at the input node: readout channel in the form of modified 3T cell, input (charge integrating) capacitance reduced by disconnecting the polysilicon plate covering the pixel cavity from the input and connecting it to a supply line

The layouts of the test structures for investigation of matching, noised and radiation hardness of transistors are illustrated in figures B.3 to B.5.

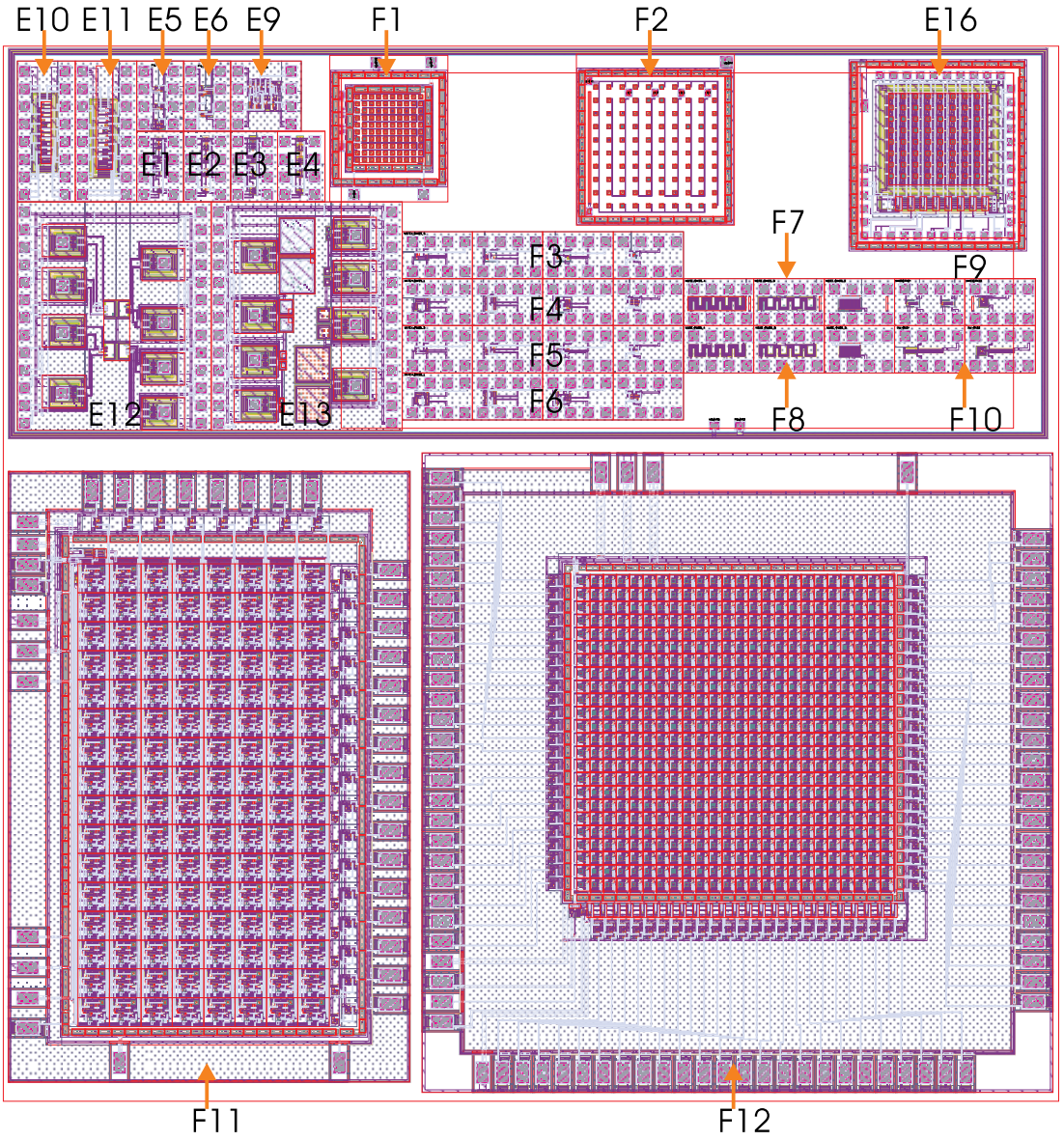


Figure B.2: General layout of the SUCIMA2 test structure.

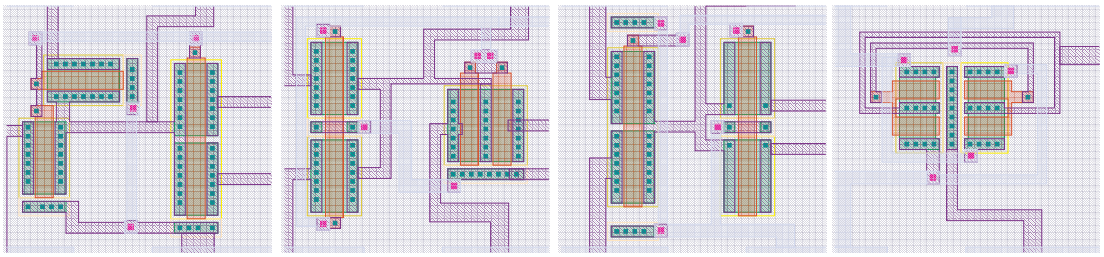


Figure B.3: Layouts of the transistor couples allowing assessment of the matching properties.

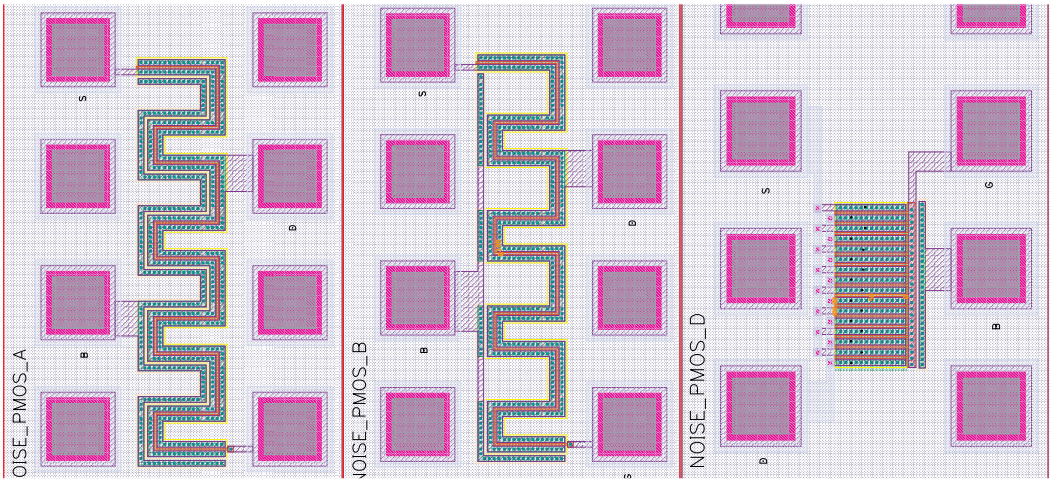


Figure B.4: Layouts of the transistor allowing assessment of the noise parameters: starting from the left structure - snake-like transistor with a bulk contact close to the source, snake-like transistor with a local bulk polarization, transistor with a comb gate.

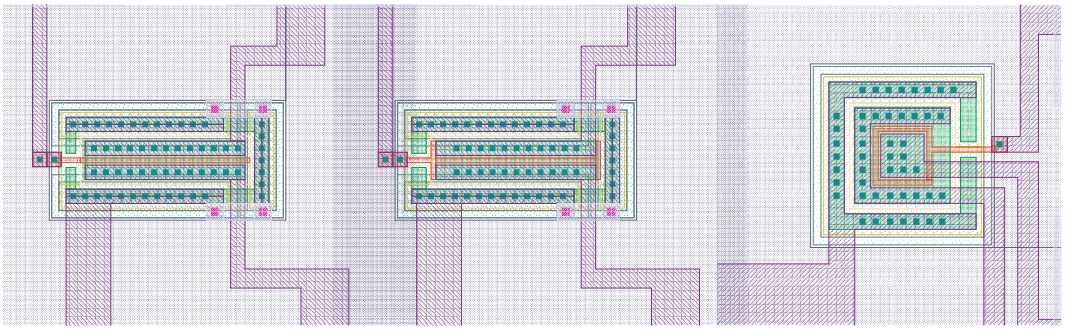


Figure B.5: Layouts of the transistor couples allowing assessment of the radiation hardness of NMOS transistors: starting from the left structure - transistor with a conventional layout, an H-gate and an enclosed geometry.

Appendix C

Test Structure for SOI Sensors in Submicron Process

The fallowing test structures are designed for the purpose of the SOI sensor development in a deep submicron process. The test structures exploit the possibility of connecting the radiation sensitive diodes with the readout electronics by tiny holes in the silicon film and BOX filled in with tungsten.

Version 1

The structure consists of a matrix of 8 by 8 pixels (connected in one chain), three guardrings and contacts to the device layer. In this test structure, the mask widths for the silicon film etching and the box etching have the same dimensions. A general view of the structure is given in figure C.1. The structure is to be produced in several versions with the pitch of 25, 50, 100 and 150 μm and the pixel implantation width of 1.5, 3 and 5 μm.

Version 2

In contrast to the previous test structure, in this design, the mask width for silicon film etching (pixel1) is wider than the mask width for box etching (pixel2). The structure is to be produced in two versions. Both versions should have the pitch of 25 μm and the pixel1 width of 5 μm. The pixel2 mask should have the width of 4 μm or 3 μm. In the first case the pixel1 extension of the pixel2 is 0.5 μm from each side, while in the second case - 1 μm from each side. A general layout of the test structure is similar to the one presented in figure C.1, but the mentioned ratio of the widths of the pixel1 and pixel2 masks is different.

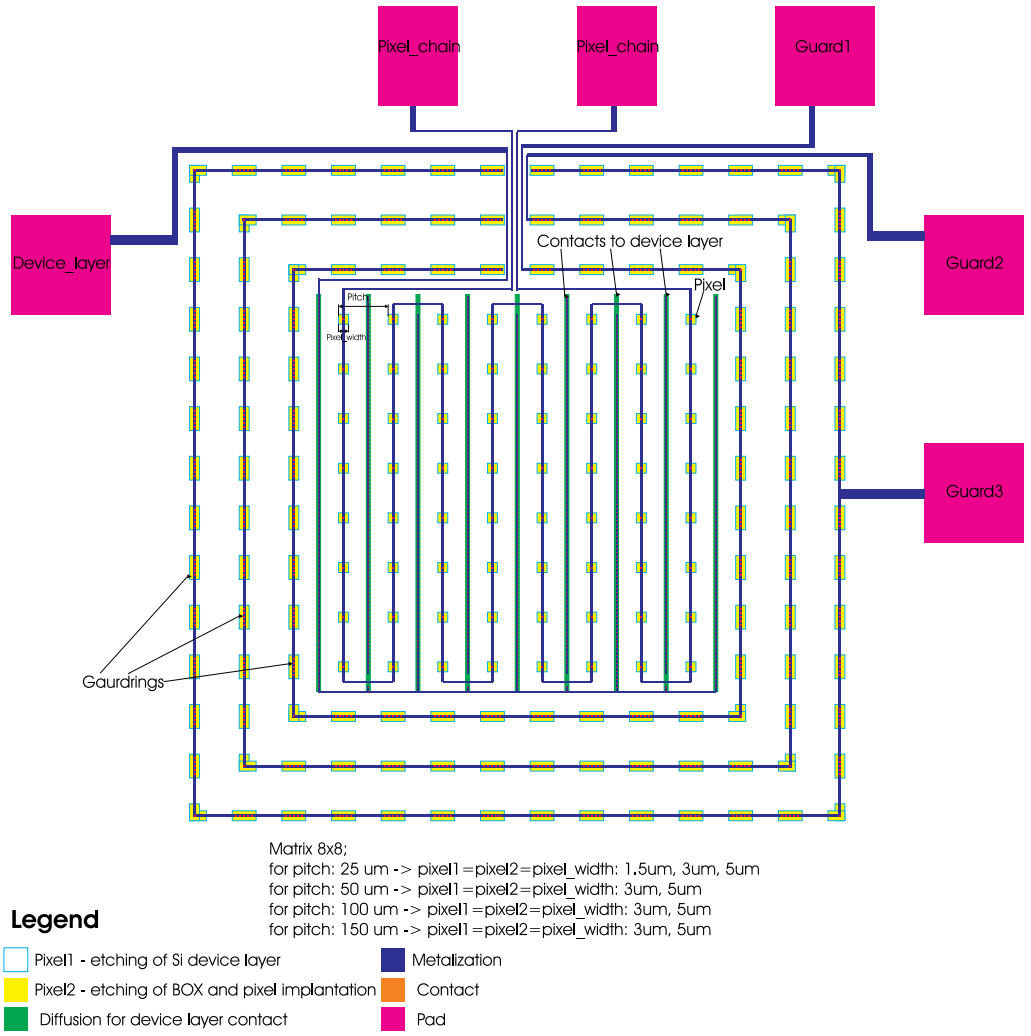


Figure C.1: Version 1 of the test structures for the development of SOI sensors in deep submicron technology.

Version 3

Last test structure is a matrix with a variable number of pixels and different pitchs. The number of pixels is equal to $k * 8 \times k * 8$, where $k = 100/pitch$ [μm]. The pixel width is constant and equal 5 μm. The structure is to be produced in several versions: with the pitch of 100 μm (then 8×8 pixels), 50 μm (then 16×16 pixels) and 25 μm (then 32×32 pixels). An example of the test structure for k=4, i.e. pitch=25 μm and 32×32 pixels is given in figure C.2.

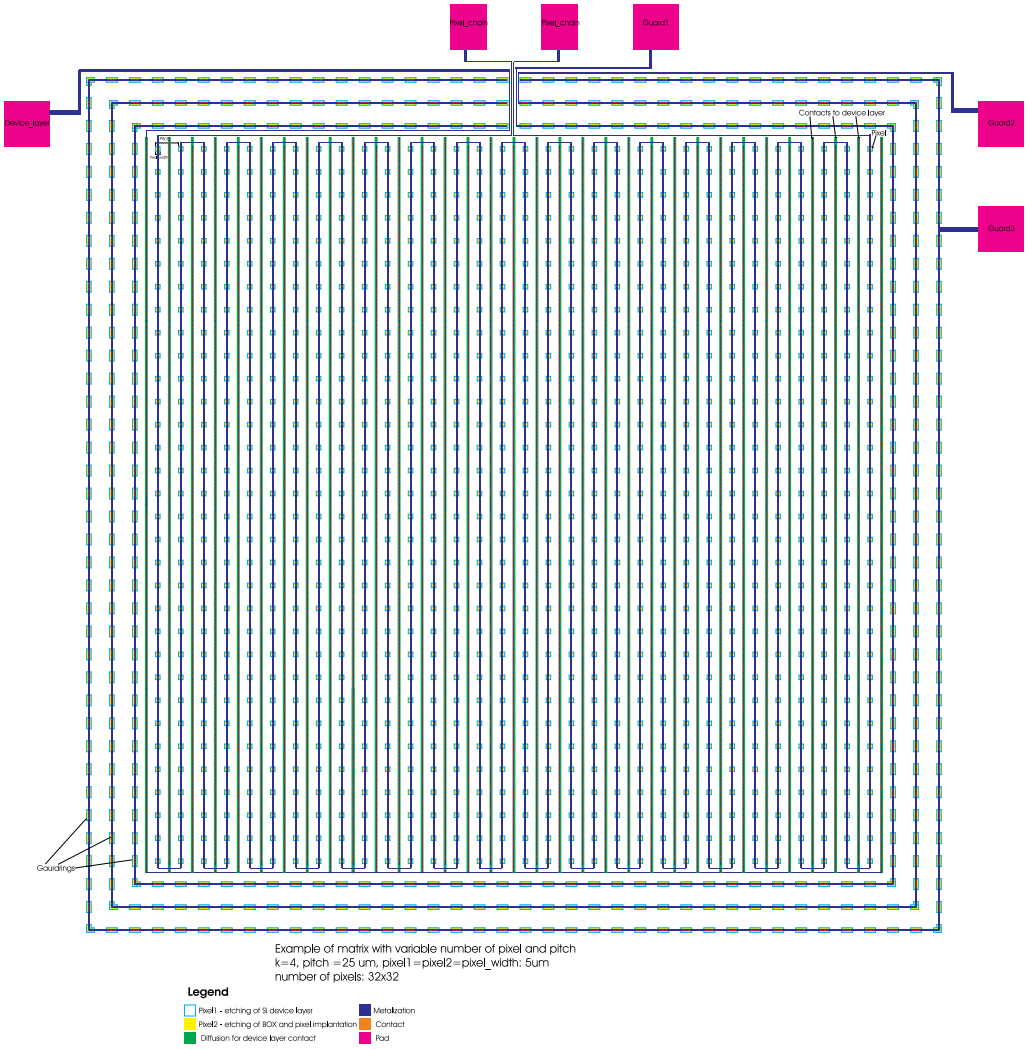


Figure C.2: Example of the test structure for the development of SOI sensors in deep submicron technology - version 3.

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